Frequency-Domain Analysis and Optimization of Microwave Class-E Power Amplifiers

by

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Abstract

Optimizing power amplifier (PA) efficiency has the added advantages of reducing size and weight, increasing reliability and operation time of radio transmitters.

At low frequencies, Class-E power amplifier (PA) demonstrates a drain efficiency close to 100%. Desirable features of Class-E PA includes, but not limited to a priori designability, high tolerance to circuit variations and excellence overall linearity. Previous analysis on Class-E circuit has been carried out in time domain. Technically speaking, lack of general analysis methods that are compatible with microwave conventions and robust enough to adapt to new load-network topology are the major obstacles hindering the development of microwave Class-E PA.

In this project, a general analysis method based on harmonic balance concept has been developed. The analysis method is capable of analyzing an arbitrary Class-E circuit independent of load-network topology choice and method of implementation. Class-E concept has been re-expressed in frequency domain and combined with the idea of harmonic tuning towards high frequency high efficiency amplification. Direct optimization is made possible by exploiting the gradient information embedded within the special structuring of the new formulation. Four solid-state power amplifiers were constructed to illustrate the simple design procedure. State-of-the-art efficiency of over 80%-90% have been achieved at L band and C band. This work lay the foundation to further analysis of microwave Class-E PA.

摘要

優化功率放大器(PA)之轉換效率將有助降低無線電傳送器之重量、大小及提升其可靠性及運作時間。

於低頻應用中，E 類 PA 展示出接近 100%之完美效率。高預先設計性、高線路誤差阻抗及優秀全面線性表現等等皆為 E 類功放之特點。文獻記載之 E 類 PA 皆以時域分法分析。E 類 PA 在微波發展之潛在最大障礙，為欠缺一套合用於微波行規而又能有效應用於其他負載拓撲之通用分析方法。

本文運用諧波平行技術，發展出一套能分析任意負載拓撲及實現方法之通用分析技術。為要達至高頻和高效率之放大，E 類觀念將首先以頻域理論重新演譯，再結合諧波調校一起使用。採用新設計方程所包含之梯度資料，本方法可做到直接優化效果。為顯示是種簡單設計程序，我們作了四個在 L 波段及 C 波段運作的固態 PA，而他們皆展示出超過 80% - 90%之超高效率。本文對未來 E 類 PA 之發展奠下重要基礎。

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Chapter 1 Introduction

Radio communication system transmits information between two points by means of an electrical signal. Radio signal encounters attenuation as it propagates through the transmission media. For reliable recovery of the original signal at the receiver side, the transmitter must pump the radio signal to a proper power level for transmission before it is buried below the noise floor. Power Amplifier (PA) is invariably the last stage in the amplifier chain for this power pumping purpose. Therefore, power level at this stage is at its maximum, which also makes power amplifier the dominant power consumer in a communication system.

Power amplifier efficiency is thus the key figure of merit to optimize. By increasing the amplifier efficiency from 50% (maximum efficiency for Class-A PA) to 90% (typical for Class-E PA at low frequencies), the dissipated heat reduced by a factor of nine for the same output power level. Hence, heat sink requirements can be greatly relaxed, which results in compact and lightweight power module. Reduction of dissipated heat has the added advantage of lowering the junction temperature rise, thereby decreasing the transistor failure rates and increasing the reliability of the power module as a whole. This together with the requirements to provide operability over extended period of time for battery powered transmitters have placed heavy premium for amplifier efficiency.

Over the years, various high efficiency amplification techniques have been proposed. The wisdom behind these techniques is very simple: Power dissipation in the output active device is characterized by simultaneous presence of voltage and current across the

device. By proper shaping of either the voltage/current waveforms or both, overlapping of voltage/current waveforms can be minimized, if not totally avoided. Different waveform shaping methods result in different modes or classes of operation such as Class-A, Class-B, Class-C, Class-D, Class-E and Class-F. Performance merits and design requirements for various classes have been addressed in the literature [1]-[3]. Different classes excel under different conditions: Class-A delivers linear amplification at the cost of low efficiency. Class-B and Class-C offer linear and high efficiency amplification suitable for non-constant envelope modulation scheme. Class-D [4] offers ultra high efficiency (ideally 100%) at low frequencies. Class-F [5]-[6] becomes the de facto high efficiency amplification techniques (typical 60%-80%, ideally 100%) at microwave frequencies.

However, to achieve 100% efficiency, ideal Class-F requires the output load network to present short circuit at all even harmonics and open circuit at all odd harmonics of the fundamental frequency at exactly the transistor output. Implementation of these mutiresonator output networks at microwave frequencies is relatively expensive [7]. Besides, at microwave frequencies, transistors are far from ideal. Finite output capacitance, lead inductance and package effects all make the implementation of reasonably ideal tuned circuits difficult. For example: lead inductance offsets the perfect short presented to the transistor at the second harmonic; finite output capacitance virtually short the transistor's output terminal at 3rd and higher harmonics. Under such conditions, differences between Class-B and Class-F narrow down and amplifier efficiency varies from 100%(ideal Class-F) to 78% (ideal Class-B)[8].

The Class-E concept introduced by Sokal in 1975, take into account of the finite output capacitance as part of the transistor model offers another means to achieve high efficiency which ideally delivers 100% efficiency. At low frequencies, such circuits demonstrated efficiency as high as 96%[9]. However, to date, most Class-E power amplifiers have been confined to low frequency applications. Among various classes of operation, Class-E is probably least understood by the microwave community. This is because conventional approach towards Class-E has been carried out in time domain. The analysis is applicable only to the specific network topology under a specific implementation method (usually using lumped elements). A change in topology requires a completely new analysis procedure which is typically long and tedious. On the other hand, classical output network for Class-E operation exhibits different problems when it is used at microwave frequencies. Both matching effects and harmonic loading effects on amplifier performance are not fully incorporated in conventional analysis.

1.1 Project Overview

Lack of a generalized analysis method precludes the migration of Class-E PA to microwave frequencies. The potential of microwave Class-E is not fully exploited in the past. Theme of the project is to:

- Devise an analysis method independent of topology choice and method of implementation.
- Rediscover many of the desirable features offered by low frequency Class-E PA.
- Exploit new features of microwave Class-E PA to the fullest extend under the generalized framework.
- Synthesize appropriate network to achieve Class-E operation.

This work began with a thorough re-investigation of Class-E PA. Harmonic-Balanced method was first proposed for the investigation of microwave Class-E PA. Both Analytic and Numerical solutions for optimum Class-E operations were derived, all based on idealized conditions. The analysis results are useful by themselves, they are also intended to be used in conjunction with other CAD and measurements techniques such as the harmonic balance and load pull methods to take into account the non-ideal behaviour of transistors at microwave frequencies. Several solid-state Class-E PAs at L-Band and C-Band were constructed through load-pull assisted design. State-of-the-art efficiency over 90% were achieved. This work lay the foundation for future investigation of microwave Class-E PA.

1.2 Thesis Organization

This thesis is organized in accordance with the main theme outlined in the previous section.

Chapter 2 begins with an overview of the Class-E concept, operation idea and its cornerstone developments. Features and limits of conventional Class-E will be explored in due course. Major obstacles towards microwave applications will then be pin-pointed.

Chapter 3 is wholly devoted to the formulation of analysis and synthesis of Class-E power amplifiers with the newly proposed Harmonic-Balanced Method, which features both topology and implementation independent characteristics.

Chapter 4 further evaluates the Class-E PA performances with the new analysis method. Effects of circuit parameter variations on PA performances will be addressed in detail.

Chapter 5 details the construction of 4 solid-state power amplifiers at L-Band and C-Band through load-pull assisted design. Performance data will also be presented in parallel with theoretical predictions.

Chapter 6 concludes this work with recommendations for future developments.

Chapter 2 Review on Classical Class-E

Classical Class-E power amplifiers offer high efficiency, a priori designability, high tolerance to circuit variations and better overall linearity than Class-B, Class-C and Class-F[10]. Yet, the past two decades has seen a proliferation of intensive research on applying Class-B, Class-C and Class-F or their variants towards high efficiency microwave amplifiers design[5]-[8],[11]-[15] , while Class-E has been largely ignored by the microwave community. Among various classes of operation, Class-E is perhaps the least well understood. This chapter serves dual purposes:

- Refresh Class-E concept, review major achievements
- Explore potentials of extending Class-E techniques to microwave frequencies.

2.1 Class-E Concept

Class-E differs distinctly from conventional PA operations in which the active device functions as a switch instead of a current source.

2.1.1 Waveform Shaping for Current-Source Active Device

Under the current source assumption, device output current is determined primarily by the input drive. Therefore the output current waveform is defined in advance. The load network is so designed such that to achieve the desired voltage waveform in response to the output current wave. For maximum efficiency, overlapping of voltage/current waveforms should be minimized.

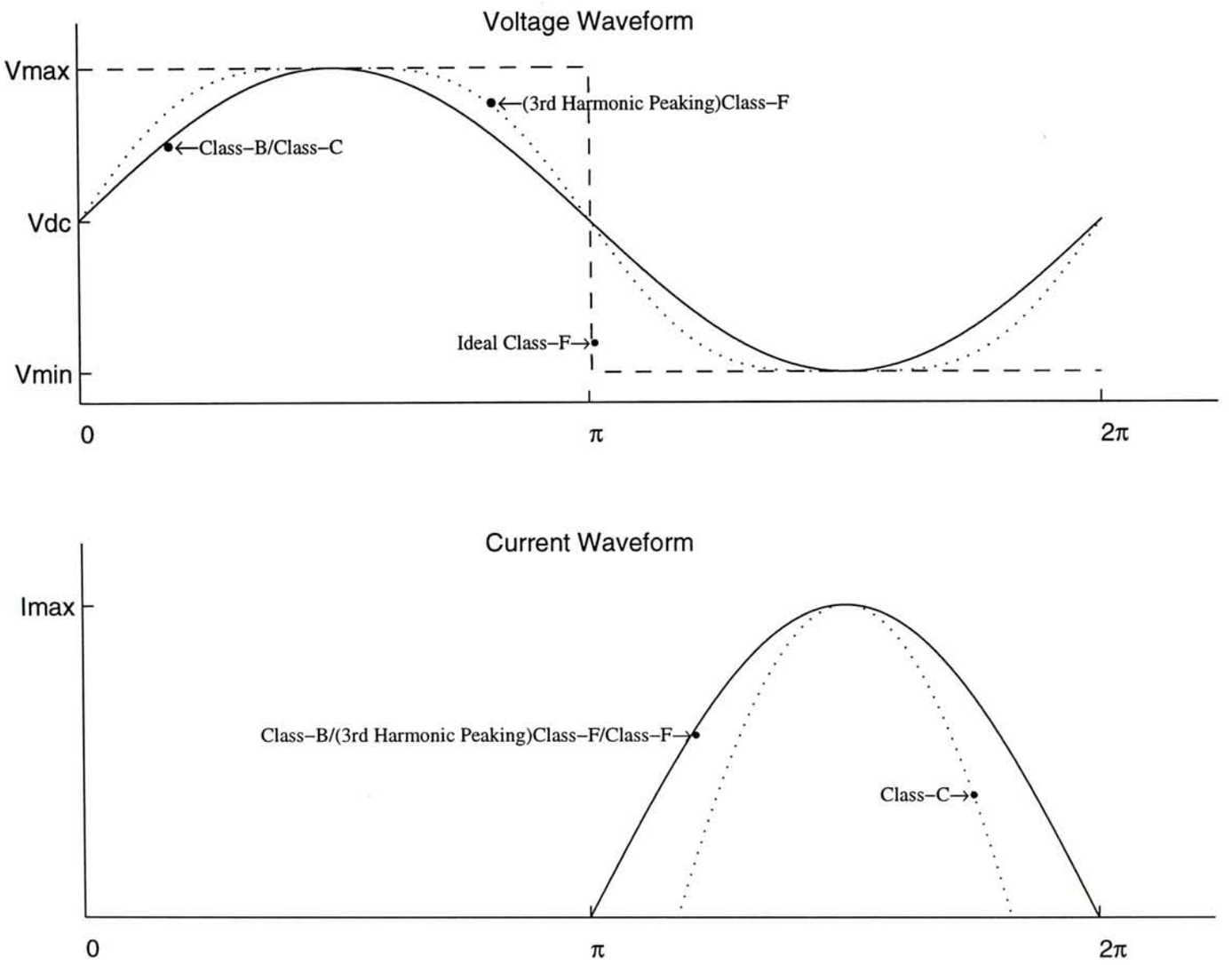


Figure2.1 Waveform shaping for active device functions as a current source

Class-B and Class-C achieve high efficiency by shaping the voltage waveform such that the minimum voltage occurs while current pulse peaks. Class-B adjusts its bias point at near threshold such that the output current is a half sine wave. Class-C further buries it bias points below the threshold , thus reducing its current pulse width.

Harmonic resonators can be added to the load network to flatten the bottom of the voltage waveform. By proper control of the 3rd harmonic component, voltage waveform flattens both at top and at bottom. This is sometimes referred as "3rd harmonic peaking Class-F" [16]. In ideal Class-F, all even harmonics are short circuited and all odd harmonics are open circuited. The resulting voltage waveform is a perfect rectangular train which ideally delivers 100% efficiency[3].

Figure 2.1 shows various waveforms under the current source assumption. Notice that V_{min} should ideally be zero. However, achievable V_{min} is dictated by the device characteristics (e.g., knee voltage in MESFETs). Bringing the bottom of voltage waveform below achievable V_{min} force the device into saturation(e.g., because of input over drive). Under saturation, device output current is no longer solely shaped by input drive, but is also strongly influenced by the load network. When that occurs, current source assumption fails and the device behaves as a switch accidentally. The load network not just shape the voltage waveform but also the current waveform as well. The amplifier operates in violation with its theoretical assumptions. Unfortunately, this always results in suboptimal, if not disastrous amplifier performance.

2.1.2 Waveform Shaping for Switch-type Active Device

While current source design approach tries to avoid device saturation, switch-type design approach takes the aggressive role of forcing the active device into saturation on purpose. Driven into saturation, the output voltage is maintained at a relatively low level while

current flows. This corresponds to a low impedance state. If the voltage tries to revert to a high level during other part of the ac cycle, the output current is shut down deliberately by driving the input below threshold. This resembles a high impedance state. By operating in this mode, the active device virtually functions as a switch. Voltage/Current waveforms are displaced in time. Increased efficiency results from reduced overlapping of voltage/current waveforms.

Figure 2.2 shows the general voltage/current waveforms associated with a switch. In contrast to current source assumption, both voltage/current waveforms are not fully defined in advance. There is no clear source of voltage or current. The voltage waveform is a function of the current waveform, which in turn is also dependent on the voltage waveform.

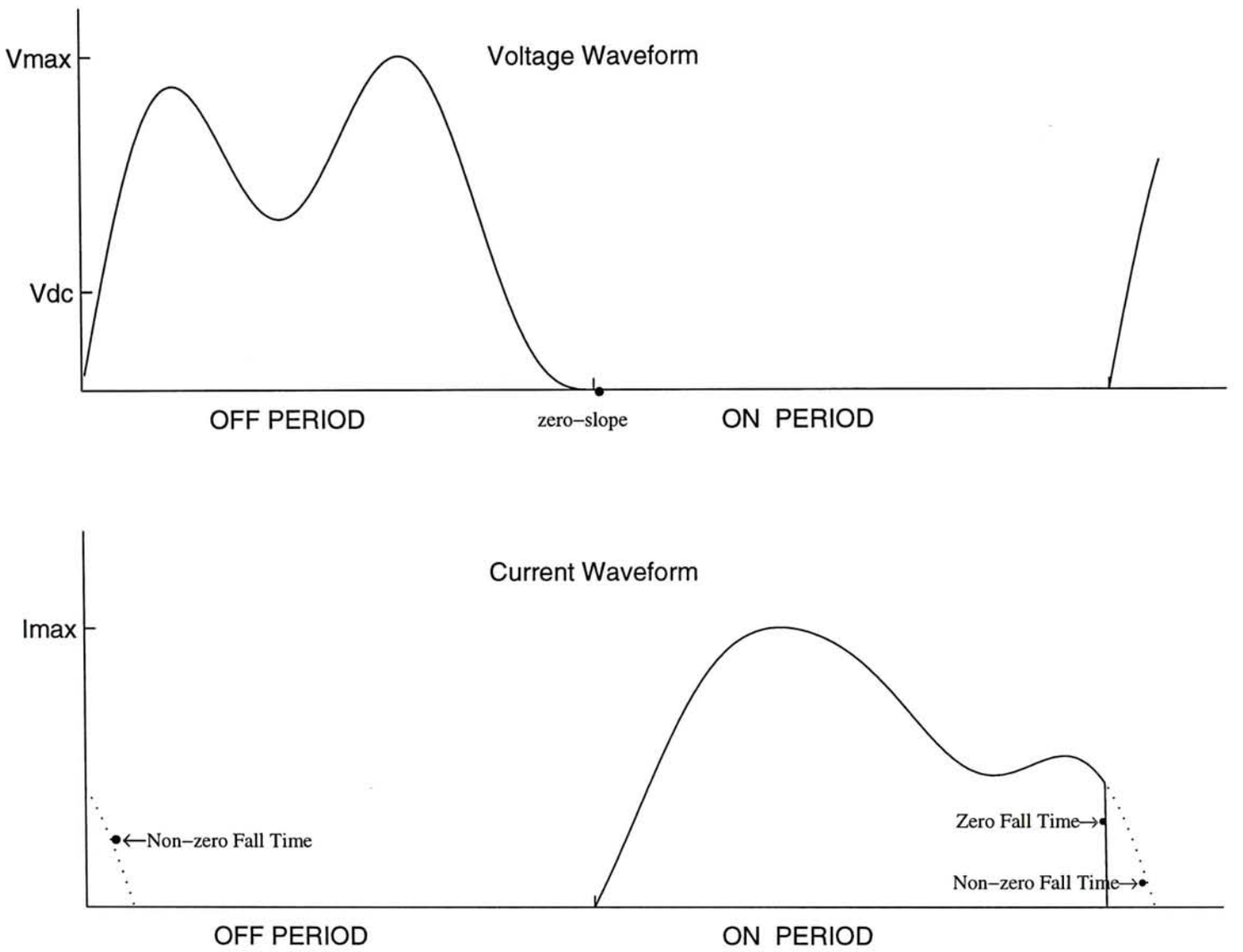


Figure 2.2 Waveform shaping for active device functions as a switch

During OFF period, the switch is shut down and there is no current passing through the device. Meanwhile, the switch derives its voltage across itself through the transient response of the load network. Voltage waveform at this state is said to be under "free-float".

During ON period, the switch is fully turned on, ideally bringing the voltage to zero. Meanwhile, transient current from the load network rushes through the switch. Current waveform at this state is said to be under "free-flow".

2.1.3 Optimum Class-E conditions

By operating the active device as a switch alone is not sufficient to achieve high efficiency. At RF and microwave frequencies, all physical devices' switching time will be appreciable fractions of the RF cycle. Unnecessary power dissipation may still exist through simultaneous presence of high voltage and high current during switching. To accommodate finite switching transitions and avoid associated losses, Sokal [9] stated 3 conditions on switch waveform shaping:

1. The rise of switch voltage at turn-off should be delayed until after the switch is off.
2. The switch voltage should resume to zero at turn-on.
3. The slope of switch voltage should be zero at turn-on

Condition 1 avoids the simultaneous imposition of substantial voltage and residual current across the switch at on-to-off transition. In case zero-current switching is not possible[17], non-zero current fall time must be tolerated with reduced efficiency.

Condition 2 avoids the losses associated with discharging the shunt output capacitor (intrinsic transistor output capacitor + external shunt capacitor). Suppose the residual voltage at turn-on is V instead of 0, each time the switch turns on, the output capacitor

with capacitance C will discharge through the switch, with associated energy loss $1/2CV^2$ per cycle, independent of discharging time constant.

Condition 3 does not directly related to efficiency enhancement. The zero-sloping condition ensures condition 2 is maintained in time neighborhood at turn-on. This permits accidental mis-tuning. In addition, zero-sloping voltage smooth out current injection at turn-on, allowing the gradual build up of transistor transconductance.

2.2 Class-E Circuit Operation

Figure 2.3 shows the circuit diagram of a widely adopted Class-E amplifier configuration. The usual active device is modeled as a switch in parallel with shunt capacitor C_{out}. C_{out} includes an external added capacitor with the parasitic output capacitor inherent in microwave transistors. The switch-capacitor combination forms the integral model of the active device as a whole. Inductor L_{RFC} bias the amplifier to V_{supply} and can be part of the ac-circuit. L_o - C_o forms the series resonant circuit tuned at fundamental frequency. jX is a fictitious circuit component representing the residual reactance of L_o - C_o at fundamental. jX shapes the voltage to desired waveforms by introducing an appropriate phase shift between the output voltage V_o (t) and the switch voltage V_s (t).

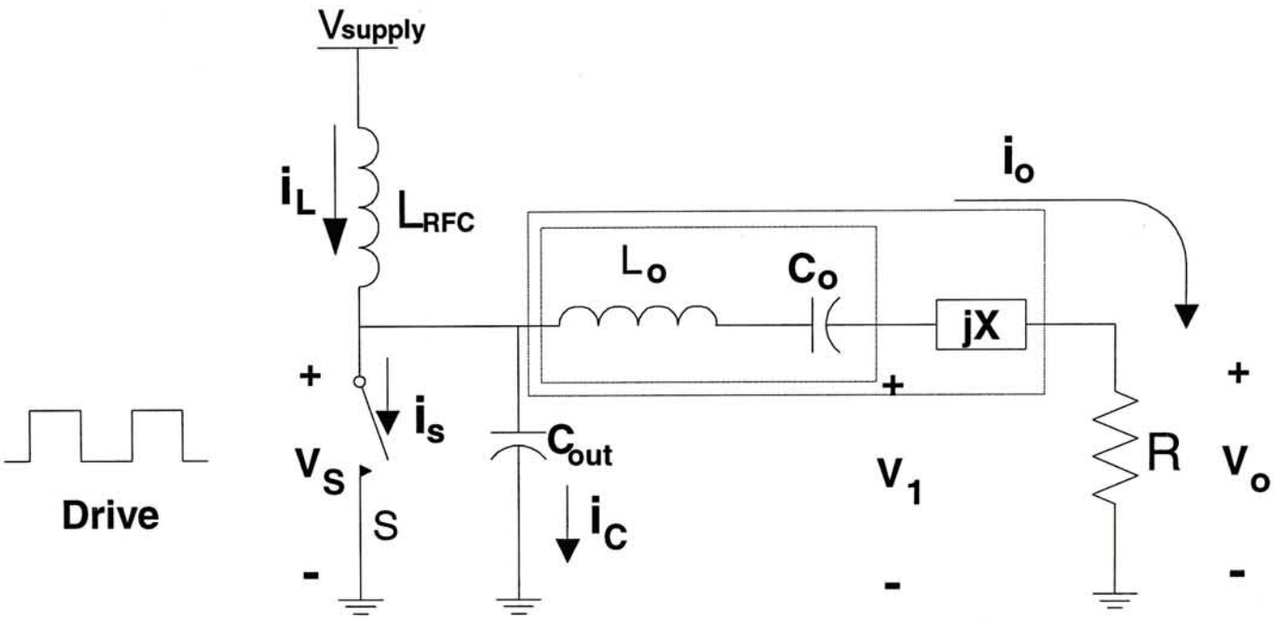


Figure 2.3 Nominal Class-E amplifier circuit

Figure 2.4 shows the corresponding waveforms associated with this circuit. A driving waveform capable of producing the desired switching action is assumed. During angular time interval (0-π), the switch is open, current through the switch is zero. During angular time interval (π-2π), the switch is closed, voltage across the switch is zero. Zero-voltage/zero-current waveforms at the corresponding period of the rf cycle is defined by the switching action, not by the load network. Meanwhile, their counterpart at the same period is derived through the transient responses with the load network. When the switch is off, current through L_{RFC} splits between the two branches containing C_{out} and R. C_{out} charges up, which forms the switch voltage. When the switch turns on, any residual charges in C_{out} will be discharged through the switch, resulting possible current spike with associated 1/2C V^2 loss per cycle. Optimum Class-E conditions can be achieved with this network by a proper design. In this case, the switch voltage resumes zero value with zero-sloping at turn-on. Under ideal situation, this amplifier delivers 100% efficiency.

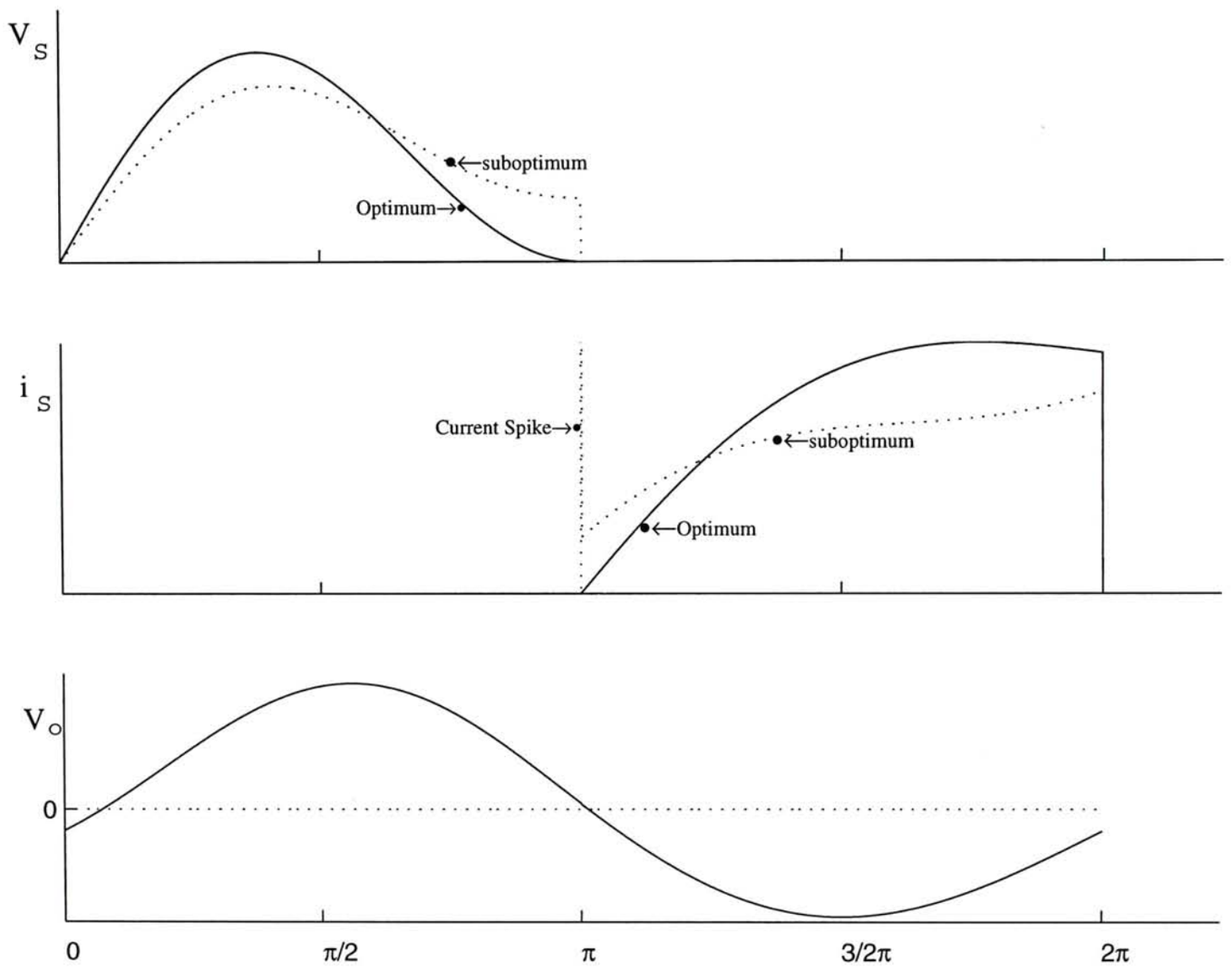


Figure 2.4 Waveforms in Class-E amplifier

2.3 Analysis and Synthesis Methods

The analysis of Class-E circuit is a non-trivial task. The exact solution of the circuit shown in Figure 2.3 involves a set of differential equations which are transcendental in nature. Numerical solution provides little insight into its operations. Network synthesis to achieve optimum Class-E conditions becomes a formidable task under general

conditions. Various assumptions are made to simplify the analysis and synthesis procedures.

2.3.1 Rabb's work

Rabb analyzed the Class-E circuit shown in Figure 2.3 based on the following assumptions[10],[18]:

1. L_{RFC} is replaced by a RF choke, which forces a dc current into the network.
2. The Q of L_o-C_o is high enough so that the load current is a pure sinusoid.
3. The switch is ideal with zero saturation voltage, zero on-resistance, infinite off-resistance and offer instantaneous switching action.
4. C_{out} is not a function of the switch voltage.
5. The switch with its represented active device can withstand negative voltage and current.

The analysis begins by assuming a sinusoidal current exists across the load (assumption 2). The RF choke forces the dc current into the network (assumption 3). The switch voltage is then expressed in terms of these two current components. Next, dc component of the switch voltage is related to the supply voltage, while the fundamental component of the switch is related to the output voltage through Fourier Series expansion. Optimum Class-E conditions (zero-voltage and zero-sloping at turn-on) are then imposed on the time equation describing the switch voltage. Optimum network parameters can be derived through careful manipulation of the nonlinear equations. Design equations for optimum Class-E amplifier under 50% duty cycle are summarized below[19]:

$$R = \frac{2}{1+\frac{\pi^2}{4}} \frac{V_{supply}^2}{P_o} \tag{2.1}$$

$$X = \frac{\pi}{8}\left(\frac{\pi^2}{2} - 2\right)R = \frac{\pi}{4}\frac{\frac{\pi^2}{2} - 2}{1+\frac{\pi^2}{4}} \frac{V_{supply}^2}{P_o} \tag{2.2}$$

$$B = \omega_o C_{out} = \frac{1}{\pi} \frac{P_o}{V_{supply}^2} \tag{2.3}$$

where ω_o = fundamental angular frequency

P_o = desired output power

2.3.2 Zulinski's work

Zulinski expanded upon Rabb's work by relaxing the RF choke assumption (assumption 1 in Rabb's work)[20]. In this case, L_{RFC} forms part of the ac circuit. Current waveform passing through L_{RFC} is unknown in advance. Similar to Rabb's work, Zulinski starts the analysis by assuming a sinusoidal output at the load. Based on conventional circuit analysis techniques, time equations governing the system in ON-state and OFF-state are formulated separately. The two set of time equations are related to each other through the boundary conditions which require that current through inductor L_{RFC} be continuous. Next, the resulting time waveforms are related to the dc supply voltage and sinusoidal output through Fourier Series expansion. Optimum Class-E conditions are imposed on corresponding time waveform, which results in optimum circuit parameters. Unlike Raab's work, the governing equations are very complex. No simple explicit design equations are available. Numerical searching methods can be employed to find the

optimum solution. However, the finite dc-feed circuit does offer the following advantages:

1. Reduced network loss due to high series resistance associated with large inductors.

2. Increased design freedom under the same bias conditions and output requirements.

3. Tradeoffs with regard to device stress, output power capability, frequency limitation and available component values can be made among various possible solutions.

4. Offers additional desirable features pending further investigation[21],[22].

2.3.3 Kazimierczuk's work

Kazimierczuk relaxed Raab's high Q assumptions on Class-E output network[23]. In this analysis, a priori waveform is not assumed at the load. Switch waveforms can no longer be related to presumed output waveforms through Fourier Series expansion. By using Laplace-transform and assuming a constant dc feed through the RF choke, time equations for various waveforms at ON-state and OFF-state are expressed in terms of the circuit Qs. Continuity requirements for voltage across capacitor C_o and current through L_o are imposed as boundary conditions relating the 2-set of time equations. Optimum circuit parameters and harmonic output spectrum are tabulated for Various Qs.

Kazimierczuk's work offers the following insights:

1. Optimum Class-E conditions can be satisfied at any Q.

2. Optimum network parameters are strong functions of Q.

3. Optimum Class-E conditions eliminate power dissipation across the active device. It does not constrain load harmonic dissipation.

4. The series tuned resonator L_o-C_o serves as an output filter, with different filtering capabilities indicated by Q. Individual harmonics are uncontrollable by this resonator.

5. Output filter for Class-E PA not only affect harmonic power level, operating bandwidth, but also the optimum network parameters and PA performances as a whole. Therefore, Class-E PA output filter cannot be designed in isolation [24]-[26].

2.3.4 Collective Efforts

With regard to Rabb's assumption 3, Raab and Sokal gave a rough estimation on performance degradation due to non-zero saturation voltage, finite on resistance and finite switching times. Later on, effects of non-zero transistor current fall time were investigated in detail by Kazimierczuk and Blanchard[28],[29]. These joint efforts allow a more accurate estimation of the dissipated power and hence more accurate circuit and thermal design.

The feasibility of using nonlinear capacitor in Class-E amplifiers as the sole output capacitor is confirmed by Chudobiak[30]. This implies that microwave Class-E operations can solely rely on the nonlinear parasitic output capacitor intrinsic to modern microwave transistors.

With the help of a digital computer, exact analysis of the Class-E circuit shown in Figure 2.3 can be achieved by using Laplace-domain approach[31],[32] or by State-Space approach[33]. These numerical methods offer powerful analysis tools, but they are not very efficient in network synthesis. Therefore, network synthesis can be accomplished through analytical approach under simplified assumptions. The optimum parameters so obtained are then analyzed by the numerical analysis tools and fine tuned if necessary. Time waveforms are checked to see if excessive negative voltage/current exists. Device stresses are checked against transistor's maximum ratings.

2.4 Additional Amplifier Configurations

Previous literature on Class-E amplifiers was mainly focused on the series tuned circuit

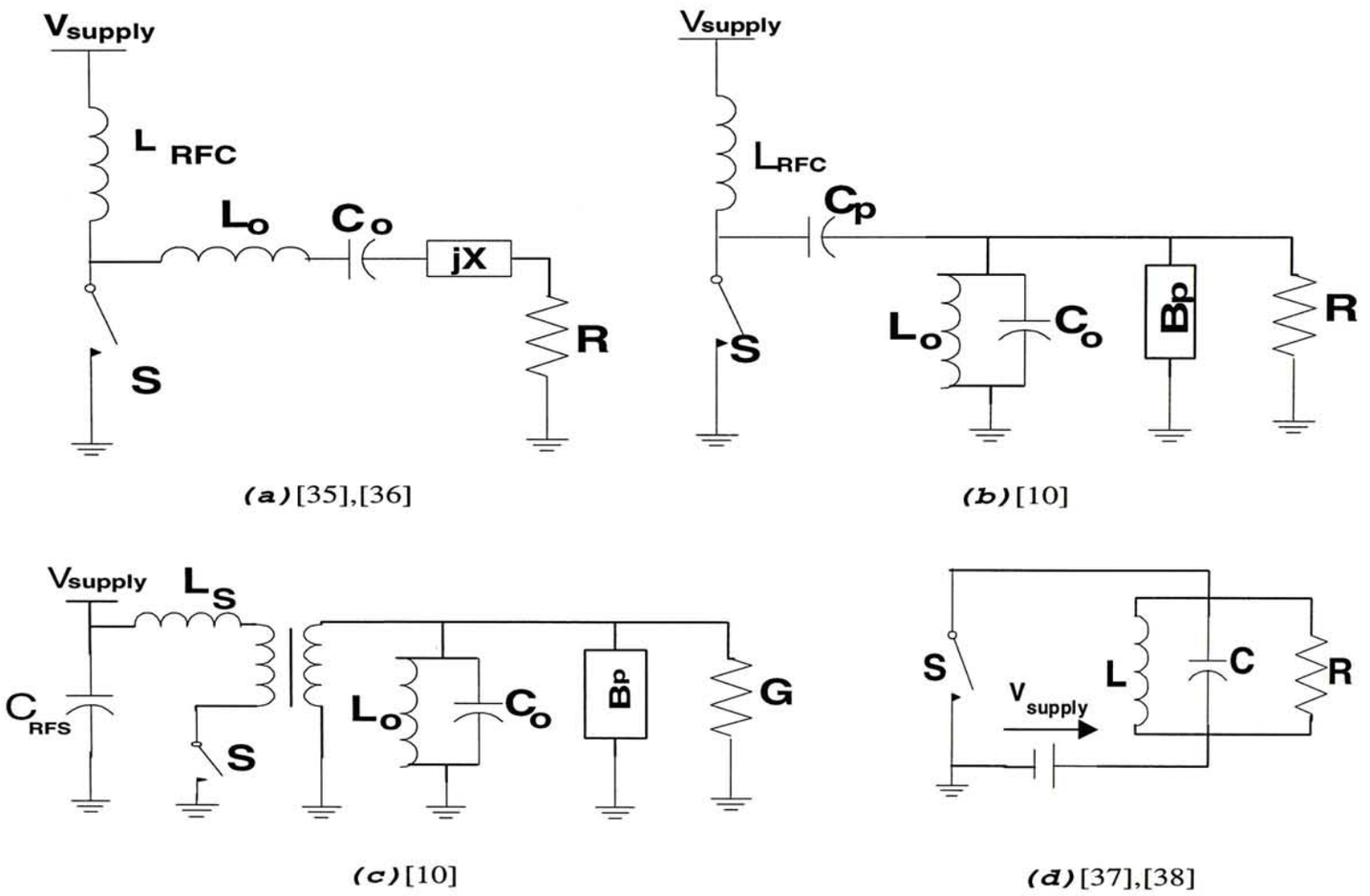


Figure 2.5 Additional Class-E configurations

configuration shown in Figure 2.3. However, physical implementation of this configuration is limited by available component range, small circuit broad area, and excessive losses associated with large inductors[34] (e.g., MMIC). Availability of various configurations to suit the adopted technology is the key to contemporary Class-E PA design. Figure 2.5 shows several single-ended Class-E configurations seen in the literature.

Figure 2.6 shows one of the new configurations studied by the author. RF choke and high Q parallel tuned resonator are assumed in this circuit. C_{out} represents external add-on capacitor with the necessary parasitic output capacitor inherent in microwave transistors. C_X blocks the dc-bias from reaching the load and absorbs the differences between switch waveforms and the desired sinusoidal output. Design information are given below in Table 2.1, 2.2 and 2.3.

Table 2.1 Set Operating Parameters

V_{supply} = DC Supply Voltage	P_o = Desired Output Power
$\frac{y}{\pi}$ = Switch Duty Ratio	$\xi = \frac{1}{V_{\text{supply}}} \left.\frac{dV_s(t)}{dt}\right\|_{turn-on}$

Table 2.2 Definition of Intermediate Variables

$R_{dc} = \frac{V_{\text{supply}}^2}{P_o}$	$g = \sqrt{2\frac{R_{dc}}{R}}$	$k = \frac{B_x}{B_{out} + B_x}$
$r_{y0} = -(RB_x - kRB_{out})(\sin y \cos y + y) + \pi RB_x$		
$r_{y1} = 2(RB_x - kRB_{out})\sin y \cos y$		
$r_{y2} = (RB_x - kRB_{out})(\sin y \cos y - y) + \pi RB_x$		

Table 2.3 Evaluation of Optimum Circuit Parameters

1a) $\beta = \tan^{-1} \dfrac{\dfrac{\sin y}{y} - \cos y}{\dfrac{\xi y}{\pi}\cos y - \left(1 + \dfrac{\xi}{\pi}\right)\sin y}$	1b) $Tpt = \dfrac{(\sin y - y\cos y)^2}{(\pi + \xi)\sin^2 y - \dfrac{\xi y}{2}\sin 2y} \dfrac{P_o}{V_{\text{supply}}^2}$	
2a) $B_{out} \le Tpt$	2b) $B_x = Tpt - B_{out}$	2c) $R = \dfrac{1}{2R_{dc}}\left(\dfrac{y}{\sin y \cos\beta\, B_x}\right)^2$
3a) $\tan\psi_p = \dfrac{gr_{y0}\cos^2\beta + gr_{y2}\sin^2\beta + 2k\sin y\sin\beta}{2k\sin y\sin\beta - gr_{y1}\sin\beta\cos\beta}$		3b) $B_p = \dfrac{\tan\psi_p}{R}$

In principle, the analysis and synthesis methods outlined in session 2.3 can be applied

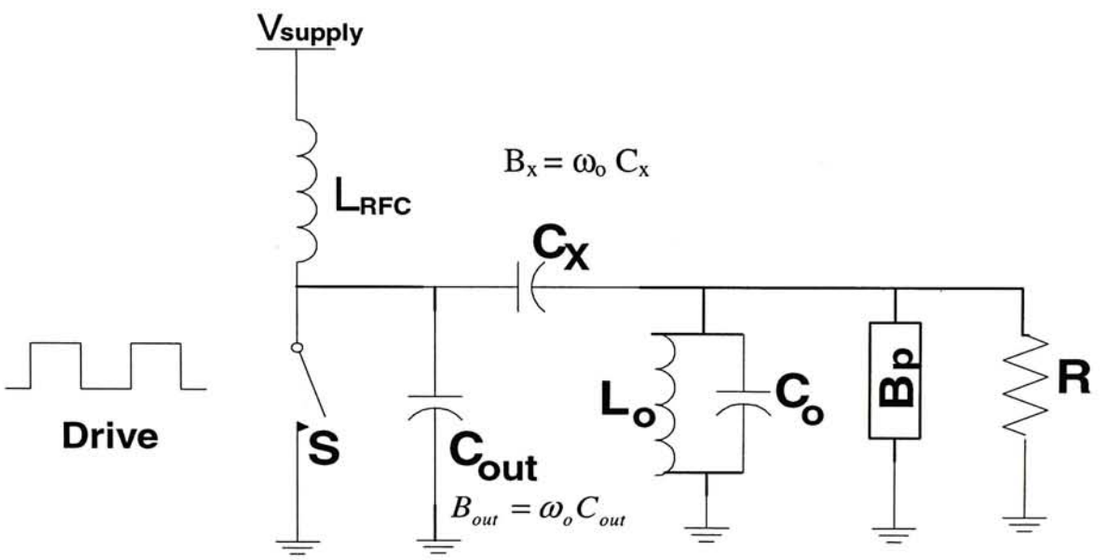


Figure 2.6 New Class-E configuration studied by the author

directly to the analysis of all these new configurations. However, the time equations governing each circuit are different. Tremendous efforts are required to arrive at a unique solution for each configuration. In our case, the design equations for the new proposed circuit were derived through months' long dedicated efforts. Therefore, generic analysis and synthesis methods are highly desirable.

2.5 Conclusion

2.5.1 Potential for Microwave Applications:

Class-E power amplifiers achieve significantly higher efficiency than for conventional Class-B or Class-C. Class-F suffers from the finite output capacitance inherent in modern microwave power transistors. In contrast, Class-E PAs are capable of incorporating the output capacitor as part of the load network.

By employing the active device as a switch, Class-E power amplifiers achieve potentially 100% efficiency. The Optimum Class-E conditions further constraint the switch voltage waveform to have zero voltage and zero-sloping at turn-on. The soft switching conditions eliminate $1/2CV^2$ loss associated with discharging the finite output capacitor and make it highly tolerable to transistor's finite switching time.

In this regard, Class-E power amplifier is fully capable of extending its operating frequency into microwave region.

2.5.2 Major Obstacles

Traditional approach to Class-E has been carried out in time domain. Derivations of analysis and synthesis equations are very involving. Dedicated efforts are required to arrive at a solution unique to specific topology. The complexity of algebra involved also limits the analysis of Class-E circuits to some very simple topology choice.

On the other hand, microwave components such as dispersive transmission lines, junction discontinuities are very difficult, if not impossible, to analyze in time domain. In

addition, the choice of topology is governed by available component range (e.g., max/min line width achievable), circuit board area, network loss concern, implementation concern (e.g., microstrips or coplanar waveguide) and choice of technology (e.g., MMIC or MIC).

In short, lack of analysis methods that are compatible with microwave conventions and robust enough to adapt to a new topology are the major obstacles hindering the growth of microwave Class-E power amplifiers.

2.5.3 Outstanding Issues

Original Class-E concept does not specify any topologies or methods for its implementation. Low frequency Class-E circuit usually uses lumped elements tuned resonators to achieve harmonic suppression. Harmonic frequency responses of distributed elements differ significantly from the simple lumped elements tuned circuit. Harmonic loading effects on Class-E PA performances have not been addressed in the past.

Besides, switch waveform shaping and Optimum Class-E conditions eliminate power dissipation across the active device. Harmonic dissipation can still exist. Additional constrains on waveform shaping are needed.

2.5.4 Requirements for new Analysis Method

Any new analysis methods should best feature the following characteristics:

- Compatible with microwave conventions, i.e., frequency domain method is preferable.
- Capable to analyze and synthesize Class-E circuit independent of topology choice and implementation methods.
- Offer additional insights into the operation of Class-E circuits.

The formulation of a new analysis method will be covered in Chapter 3.

Chapter 3 New Theoretical Development

This chapter details the formulation of a new method for the analysis of Class-E circuit based on the harmonic balance techniques. In contrast to conventional analysis methods, a priori circuit topology is not assumed. Circuit performances are expressed in terms of the load network input port voltage/current waves. The voltage/current waves are harmonic balanced analytically with the switching action. The load network input port voltage/current are related to each other through its input port load impedance as well as the switch characteristics. Given the switch operating parameters, a knowledge of the DC bias information and load network input port impedance fully characterize the system.

The structure of the formulation can be further re-constructed to accommodate the Optimum Class-E conditions or other constraints on waveform shaping. Optimum load impedance can be evaluated directly independent of the topology choice for their realization.

3.1 Basic Formulation

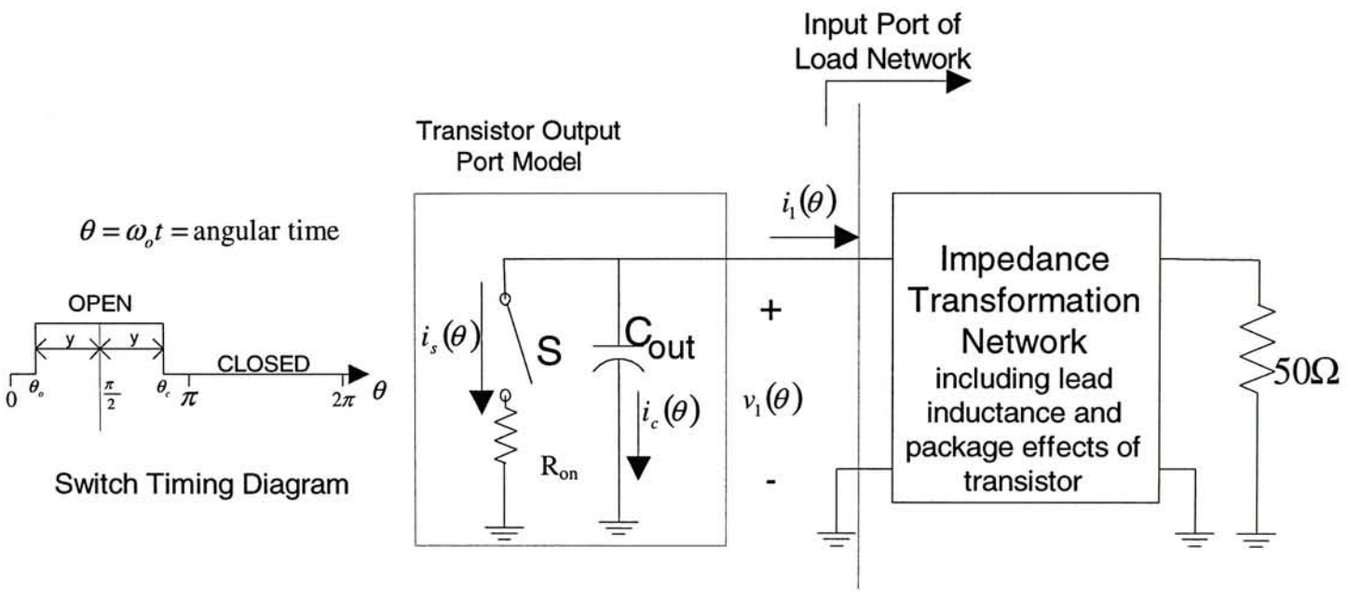


Figure 3.1 General Class-E circuit

Figure 3.1 shows the equivalent Class-E circuit. The transistor output port is modeled by an ideal switch in series with a small turn-on resistor, R_{on}. R_{on} represents the session of I-V curves to the left of the knee voltage in FET or saturation voltage in BJT for which Class-E circuit transverse during the ON period. The inclusion of R_{on} better models the transistor loss under low supply voltage. C_{out} represents the necessary output capacitor inherent in microwave power transistors.

The switch timing diagram is also shown alongside the circuit diagram. Angular time θ is used throughout the thesis for mathematical convenience. θ_o indicates the time at which the switch opens while θ_c denotes the times at which the switch closes. θ_o and θ_c also relates to the half off-time y through $\theta_o = \frac{\pi}{2} - y$ and $\theta_c = \frac{\pi}{2} + y$. Note the periodic

nature of the timing diagram, θ_o and θc are equivalent to $2\pi+\theta_o$ and $2\pi+\theta_c$ respectively. Should ambiguity arises, subscripts ON and OFF will be added to the corresponding variables to clarify whether they represent waveforms at ON period or OFF period.

The analysis is based on the following assumptions:

1. The switch is ideal with instantaneous switching transitions.

2. The output capacitor is independent of the switch voltage.

3. The transistor represented by the switch can withstand negative voltage/current.

4. The voltage/current at the input port of the load network can be represented by their Fourier Series and can be approximated by their corresponding truncated series.

3.1.1 Set up Time Equations

Assume $i_1(\theta)$ and $v_1(\theta)$ can be expressed by their Fourier Series expansion.

$$i_1(\theta)=\sum_{m=-\infty}^{\infty} I_{1m}e^{jm\theta} \tag{3.1a}$$

$$v_1(\theta)=-\sum_{n=-\infty}^{\infty} V_{1n}e^{jn\theta} \tag{3.1b}$$

During OFF PERIOD, the switch is opened:

$$i_c(\theta)+i_1(\theta)=0$$

$$\Rightarrow \qquad i_c(\theta)=-i_1(\theta)=-\sum_{m=-\infty}^{\infty} I_{1m}e^{jm\theta} \tag{3.2}$$

i_c charges up the output capacitor and gives rise to the switch voltage:

$$v_{1OFF}(\theta)=\frac{1}{B}\int_{\theta_o}^{\theta} i_c(\vartheta)d\vartheta+v_1(\theta_o) \tag{3.3a}$$

$$\text{where } B=\omega_o C_{out} \tag{3.3b}$$

Substituting (3.2) into (3.3a) and performing the necessary integration gives:

$$v_{1OFF}(\theta)=-\frac{\theta-\theta_o}{B}I_{10}-\sum_{\substack{m=-\infty \\ m\neq 0}}^{\infty}\frac{e^{jm\theta}-e^{jm\theta_o}}{jmB}I_{1m}+v_1(\theta_o) \tag{3.3c}$$

where $v_1(\theta_o)$ = initial condition inherent from the ON period.

During ON PERIOD,

$$i_c(\theta)+i_s(\theta)+i_1(\theta)=0$$

$$\Rightarrow \qquad B\frac{dv_{1ON}(\theta)}{d\theta}+\frac{v_{1ON}(\theta)}{R_{on}}=-\sum_{m=-\infty}^{\infty} I_{1m}e^{jm\theta} \tag{3.4}$$

Solution to (3.4) is given by:

$$v_{1ON}(\theta)=v_1(\theta_c)e^{-\frac{\theta-\theta_c}{BR_{on}}}-\left(1-e^{-\frac{\theta-\theta_c}{BR_{on}}}\right)R_{on}I_{10}+\sum_{\substack{m=-\infty \\ m\neq 0}}^{\infty}\frac{R_{on}\left(e^{-\frac{\theta-\theta_c}{BR_{on}}+jm\theta_c}-e^{jm\theta_c}\right)}{1+jmBR_{on}}I_{1m} \tag{3.5}$$

where $v_1(\theta_c)$=initial condition inherent from the OFF period.

$v_1(\theta_o)$ and $v_1(\theta_c)$ can be solved through the boundary conditions which require that voltage across capacitor be continuous, i.e.,

$$v_{1OFF}(\theta_c) = v_1(\theta_c) \tag{3.6a}$$

$$v_{1ON}(2\pi + \theta_o) = v_1(\theta_o) \tag{3.6b}$$

Substitute (3.6a) & (3.6b) into (3.3c) & (3.5) and solve the simultaneous equations for $v_1(\theta_o)$ and $v_1(\theta_c)$ gives:

$$v_1(\theta_o) = -\frac{\left(1-e^{-\alpha}\right)R_{on} + \frac{\theta_c - \theta_o}{B}e^{-\alpha}}{1-e^{-\alpha}} I_{10}$$

$$+\frac{\sum_{\substack{m=-\infty \\ m\neq 0}}^{\infty} \left\{ \frac{R_{on}}{1+jmBR_{on}} \left[e^{-\alpha + jm\theta_c} - e^{jm\theta_o} \right] - \frac{e^{-\alpha}}{jmB} \left[e^{jm\theta_c} - e^{jm\theta_o} \right] \right\}}{1-e^{-\alpha}} I_{1m} \tag{3.7a}$$

$$v_1(\theta_c) = -\frac{\left(1-e^{-\alpha}\right)R_{on} + \frac{\theta_c - \theta_o}{B}}{1-e^{-\alpha}} I_{10}$$

$$+\frac{\sum_{\substack{m=-\infty \\ m\neq 0}}^{\infty} \left\{ \frac{R_{on}}{1+jmBR_{on}} \left[e^{-\alpha + jm\theta_c} - e^{jm\theta_o} \right] - \frac{e^{jm\theta_c} - e^{jm\theta_o}}{jmB} \right\}}{1-e^{-\alpha}} I_{1m} \tag{3.7b}$$

where $$\alpha = \frac{2\pi + \theta_c - \theta_o}{BR_{on}} \tag{3.7c}$$

3.1.2 Complex Fourier Series Decomposition:

With (3.7a) & (3.7b) , Complex Fourier Coefficients of $v_1(\theta)$ which consists of $v_{1OFF}(\theta)$ and $v_{1ON}(\theta)$ may then be evaluated by:

$$V_{10} = \frac{1}{2\pi}\int_{\theta=\theta_o}^{\theta_c} v_{1ON}(\theta)d\theta + \frac{1}{2\pi}\int_{\theta=\theta_c}^{2\pi+\theta_o} v_{1OFF}(\theta)d\theta \tag{3.8a}$$

$$V_{1n} = \frac{1}{2\pi}\int_{\theta=\theta_o}^{\theta_c} v_{1ON}(\theta)e^{-jn\theta}d\theta + \frac{1}{2\pi}\int_{\theta=\theta_c}^{2\pi+\theta_o} v_{1OFF}(\theta)e^{-jn\theta}d\theta \tag{3.8b}$$

for n ≠ 0

After a lengthy and tedious algebraic manipulations, the coefficients of $v_1(\theta)$ may then be related to the complex Fourier coefficients of $i_1(\theta)$ through:

$$\begin{bmatrix} \vec{\mathbf{V}}_1 \\ V_{10} \\ \vec{\mathbf{V}}_1^* \end{bmatrix} = \begin{bmatrix} \mathbf{S} & \mathbf{XI} & \mathbf{T} \\ \mathbf{XV} & XO & \mathbf{XV}^* \\ \mathbf{T}^* & \mathbf{XI}^* & \mathbf{S}^* \end{bmatrix} \begin{bmatrix} \vec{\mathbf{I}}_1 \\ I_{10} \\ \vec{\mathbf{I}}_1^* \end{bmatrix} \tag{3.9}$$

where

$$\vec{\mathbf{V}}_1 = [V_{11} \quad V_{12} \quad V_{13} \quad V_{14} \quad \cdots \quad V_{1N}]^T$$
$$\vec{\mathbf{I}}_1 = [I_{11} \quad I_{12} \quad I_{13} \quad I_{14} \quad \cdots \quad I_{1M}]^T$$
$$\mathbf{S} = [S_{nm}], \quad \mathbf{T} = [T_{nm}] \quad \begin{cases} m \in \{1,2,3,4,\cdots M\} \\ n \in \{1,2,3,4,\cdots N\} \end{cases}$$
$$\mathbf{XI} = [XI_{n1}], \quad \mathbf{XV} = [XV_{1m}]$$

and

$$XO = -\frac{1}{2\pi}\left[\frac{(\theta_c - \theta_o)^2}{B}\left(\frac{1}{2} + \frac{e^{-\alpha}}{1-e^{-\alpha}}\right) + (2\pi + \theta_c - \theta_o)R_{on}\right] \tag{3.10a}$$

$$XI_n = \frac{1}{2\pi}\left[-\frac{1}{n^2 B}\left(e^{-jn\theta_c} - e^{-jn\theta_o}\right) + \frac{\theta_c - \theta_o}{jnB}\frac{1}{1+jnBR_{on}}\frac{1}{1-e^{-\alpha}}\left(e^{-jn\theta_c} - e^{-\alpha - jn\theta_o}\right)\right] \quad (3.10b)$$

$$XV_m = \frac{1}{2\pi}\left[\frac{1}{m^2 B}\left(e^{jm\theta_c} - e^{jm\theta_o}\right) - \frac{\theta_c - \theta_o}{jmB}\frac{1}{1+jmBR_{on}}\frac{1}{1-e^{-\alpha}}\left(e^{-\alpha + jm\theta_c} - e^{jm\theta_o}\right)\right] \quad (3.10c)$$

$$\begin{aligned} S_{nn} = -\frac{1}{2\pi}\Bigg\{ & \left[\frac{1}{n^2 B} + \frac{2R_{on} + jnBR_{on}^2}{jn(1+jnBR_{on})^2}\right]\frac{e^{-\alpha}}{1-e^{-\alpha}}\left[1 - e^{jn(\theta_c - \theta_o)}\right] \\ & + \left[\frac{1}{n^2 B} + \frac{2R_{on} + jnBR_{on}^2}{jn(1+jnBR_{on})^2}\right]\frac{1}{1-e^{-\alpha}}\left[1 - e^{-jn(\theta_c - \theta_o)}\right] \\ & + (2\pi + \theta_o - \theta_c)\frac{R_{on}}{1+jnBR_{on}} + \frac{\theta_c - \theta_o}{jnB}\Bigg\} \end{aligned} \quad (3.10d)$$

$$\begin{aligned} T_{nn} = \frac{1}{2\pi}\Bigg[& \frac{1}{n^2 B}\left(\frac{1}{2} + \frac{e^{-\alpha}}{1-e^{-\alpha}}\right)\left(e^{-jn\theta_c} - e^{-jn\theta_o}\right)^2 - \frac{1}{jn}\frac{R_{on}}{1-jnBR_{on}}\frac{e^{-j2n\theta_c} - e^{-j2n\theta_o}}{2} \\ & - \frac{j}{n}\frac{R_{on}}{1-jnBR_{on}}\frac{e^{-\alpha - jn\theta_c} - e^{-jn\theta_o}}{1-e^{-\alpha}}\left(e^{-jn\theta_c} - e^{-jn\theta_o}\right) \\ & + \frac{R_{on}}{jn(1+n^2 B^2 R_{on}^2)}\frac{e^{-jn\theta_c} - e^{-\alpha - jn\theta_o}}{1-e^{-\alpha}}\left(e^{-jn\theta_c} - e^{-jn\theta_o}\right)\Bigg] \end{aligned} \quad (3.10e)$$

$$\begin{aligned} S_{nm} = \frac{1}{2\pi}\Bigg[& \frac{e^{j(m-n)\theta_c} - e^{j(m-n)\theta_o}}{m(m-n)B} + e^{jm\theta_o}\frac{e^{-jn\theta_c} - e^{-jn\theta_o}}{mnB} \\ & - \frac{R_{on}}{1+jmBR_{on}}\frac{e^{-\alpha + jm\theta_c} - e^{jm\theta_o}}{1-e^{-\alpha}}\frac{e^{-jn\theta_c} - e^{-jn\theta_o}}{jn} \\ & - \frac{e^{-\alpha}}{1-e^{-\alpha}}\frac{e^{jm\theta_c} - e^{jm\theta_o}}{mnB}\left(e^{-jn\theta_c} - e^{-jn\theta_o}\right) \end{aligned}$$

$$+\frac{R_{on}}{1+jmBR_{on}}\frac{BR_{on}}{1+jnBR_{on}}\frac{e^{-\alpha+jm\theta_c}-e^{jm\theta_o}}{1-e^{-\alpha}}\left(e^{-jn\theta_c}-e^{-\alpha-jn\theta_o}\right)$$

$$-\frac{R_{on}}{1+jnBR_{on}}\frac{e^{jm\theta_c}-e^{jm\theta_o}}{jm}\frac{e^{-jn\theta_c}-e^{-\alpha-jn\theta_o}}{1-e^{-\alpha}}$$

$$+\frac{R_{on}}{1+jmBR_{on}}\frac{BR_{on}}{1+jnBR_{on}}e^{jm\theta_c}\left(e^{-jn\theta_c}-e^{-\alpha-jn\theta_o}\right)$$

$$+\frac{R_{on}}{1+jmBR_{on}}\frac{e^{j(m-n)\theta_c}-e^{j(m-n)\theta_o}}{j(m-n)}\Bigg] \qquad (3.10f)$$

for $n \neq m$

$$T_{nm} = S_{n(-m)} \qquad (3.10g)$$

for $n \neq m$

Note that since $v_1(\theta)$ and $i_1(\theta)$ are real, negative frequency components are just the complex conjugate of their positive frequency counterparts. $\vec{\mathbf{V}}_1^{\,*}$ and $\vec{\mathbf{I}}_1^{\,*}$ denote the negative frequency components of $v_1(\theta)$ and $i_1(\theta)$ in (3.9). For notational consistence, * and superscript "T" will be reserved to denote the complex conjugate and matrix transpose operations respectively throughout the thesis.

3.2 General Analysis

(3.9) relates the load network input port voltage and current through the switching matrix in frequency domain. Should the input port impedance and bias information be given , the complete system can be characterized. Load variations and Harmonic loading effects on Class-E circuit performances can also be investigated.

3.2.1 Load Network Coupling

Decomposed (3.9) into two equations:

$$\begin{bmatrix} \vec{\mathbf{V}}_1 \\ \vec{\mathbf{V}}_1^* \end{bmatrix} = \begin{bmatrix} \mathbf{S} & \mathbf{T} \\ \mathbf{T}^* & \mathbf{S}^* \end{bmatrix} \begin{bmatrix} \vec{\mathbf{I}}_1 \\ \vec{\mathbf{I}}_1^* \end{bmatrix} + I_{10} \begin{bmatrix} \mathbf{XI} \\ \mathbf{XI}^* \end{bmatrix} \tag{3.11a}$$

$$V_{10} = \begin{bmatrix} \mathbf{XV} & \mathbf{XV}^* \end{bmatrix} \begin{bmatrix} \vec{\mathbf{I}}_1 \\ \vec{\mathbf{I}}_1^* \end{bmatrix} + XO \cdot I_{10} \tag{3.11b}$$

Re-arrange (3.11b) for I_{10} ,

$$I_{10} = \frac{1}{XO} V_{10} - \frac{1}{XO} \begin{bmatrix} \mathbf{XV} & \mathbf{XV}^* \end{bmatrix} \begin{bmatrix} \vec{\mathbf{I}}_1 \\ \vec{\mathbf{I}}_1^* \end{bmatrix} \tag{3.11c}$$

Substitute (3.11c) into (3.11a) gives:

$$\begin{bmatrix} \vec{\mathbf{V}}_1 \\ \vec{\mathbf{V}}_1^* \end{bmatrix} = \left\{ \begin{bmatrix} \mathbf{S} & \mathbf{T} \\ \mathbf{T} & \mathbf{S} \end{bmatrix} - \frac{1}{XO} \begin{bmatrix} \mathbf{XI} \\ \mathbf{XI}^* \end{bmatrix} \begin{bmatrix} \mathbf{XV} & \mathbf{XV}^* \end{bmatrix} \right\} \begin{bmatrix} \vec{\mathbf{I}}_1 \\ \vec{\mathbf{I}}_1^* \end{bmatrix} + \frac{V_{10}}{XO} \begin{bmatrix} \mathbf{XI} \\ \mathbf{XI}^* \end{bmatrix} \tag{3.12}$$

(3.12) relates ac voltage/current to the DC biasing voltage. Meanwhile, the ac

voltage/current relationship is also governed by the input port load impedance. i.e.

$$\begin{bmatrix} \vec{\mathbf{V}}_1 \\ \vec{\mathbf{V}}_1^* \end{bmatrix} = \begin{bmatrix} \mathbf{Z}_L & \mathbf{0} \\ \mathbf{0} & \mathbf{Z}_L^* \end{bmatrix} \begin{bmatrix} \vec{\mathbf{I}}_1 \\ \vec{\mathbf{I}}_1^* \end{bmatrix} \tag{3.13}$$

where $\mathbf{0}$ = NxN zero matrix

$\mathbf{Z_L}$ = harmonic load impedance matrix given by:

$$\mathbf{Z}_L = \begin{bmatrix} Z(\omega_o) & 0 & 0 & \cdots & 0 \\ 0 & Z(2\omega_o) & & & \cdot \\ 0 & \cdot & Z(3\omega_o) & & \cdot \\ \cdot & & & & \\ \cdot & \cdot & & & \cdot \\ \cdot & & & & \\ 0 & 0 & 0 & \cdot & Z(N\omega_o) \end{bmatrix} \tag{3.14}$$

Solve (3.12) & (3.13) for the current vector:

$$\begin{bmatrix} \vec{\mathbf{I}}_1 \\ \vec{\mathbf{I}}_1^* \end{bmatrix} = \frac{V_{10}}{XO} \begin{bmatrix} \mathbf{P} & \mathbf{Q} \\ \mathbf{Q}^* & \mathbf{P}^* \end{bmatrix}^{-1} \begin{bmatrix} \mathbf{XI} \\ \mathbf{XI}^* \end{bmatrix} \tag{3.15a}$$

where $$\mathbf{P} = \mathbf{Z}_L - \mathbf{S} + \frac{1}{XO} \mathbf{XI}\,\mathbf{XV} \tag{3.15b}$$

$$\mathbf{Q} = -\mathbf{T} + \frac{1}{XO}\ \mathbf{XI}\ \ \mathbf{XV}^* \tag{3.15c}$$

Make use of the conjugate properties, the matrix inverse operation can be performed in modular form which results in much faster evaluation. (3.15) can hence be evaluated by:

$$\vec{\mathbf{I}}_1 = \frac{V_{10}}{XO} \begin{bmatrix} \left[\mathbf{P} - \mathbf{Q}(\mathbf{P}^*)^{-1}\mathbf{Q}^*\right]^{-1} & \left[\mathbf{Q}^* - \mathbf{P}^*\mathbf{Q}^{-1}\mathbf{P}\right]^{-1} \end{bmatrix} \begin{bmatrix} \mathbf{XI} \\ \mathbf{XI}^* \end{bmatrix} \tag{3.16}$$

When the number of harmonics to be considered is high, say greater than 8, evaluation of

$\mathbf{Q}^{-1}$ in (3.16) becomes badly scaled. Under that circumstance, $\vec{\mathbf{I}}_1$ can be solved by (3.15a). However, since semiconductor device only approximates an ideal switch, considerations of harmonics less than 8 is adequate and (3.16) is preferable to (3.15a).

Once $\vec{\mathbf{I}}_1$ has been solved, I_{10} and $\vec{\mathbf{V}}_1$ can be obtained from (3.11c) and (3.11a) respectively. Time waveforms are obtainable through inverse discrete Fourier transform (IDFT). Other derived quantities such as output power, harmonic spectrum and efficiency can be evaluated accordingly.

To summarize, the formulation can be used to analyze a switch-capacitor combination associated with any load network in frequency domain. The steps to complete frequency domain analysis are outlined below:

1. Given dc voltage bias V_{10} (system specification) and Switch-Capacitor parameter R_{on} & C_{out} (transistor parameters)

2. Evaluate the harmonic load impedance matrix for a given circuit or construct load impedance matrix for harmonic loading and load variations study.

3. Solve $\vec{\mathbf{I}}_1$, I_{10} and $\vec{\mathbf{V}}_1$ through (3.16), (3.11c) and (3.11a).

4. Time domain waveforms are obtainable through inverse discrete Fourier transform.

5. Evaluate other derived quantities such as output power, efficiency and harmonic dissipation.

3.2.2 Numerical Verification

To verify the derivations obtained, simulation results using the proposed frequency domain methods are compared with time domain simulation.

The comparisons are made using the circuit shown in Figure 3.2.

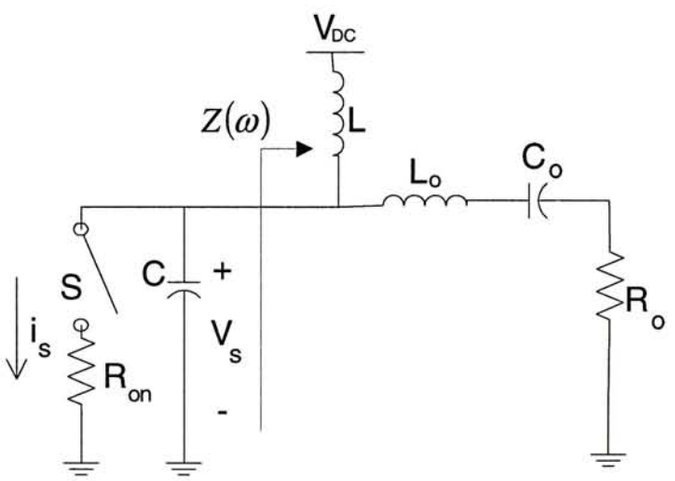


Figure 3.2 Series Tuned Class-E circuit

The comparisons are made under three different cases listed in Table 3.1

In all cases, the circuit operates at 5V DC bias with 50% duty cycle. The operating frequency is set at 1kHz.

Exact solutions to the circuit in Figure 3.2 can be obtained through the periodic steady state simulation using the state-space approach described in [33]. The frequency domain simulation is the direct application of the formulation described in the previous section.

Table 3.1 Circuit parameters used in simulations

Parameters	Values of circuit parameter under different cases		
	A	b	c
R_{on}	50Ω	0.05Ω	1.0Ω
C	27.9nF	18.085nF	7.7nF
L	99.9μH	98.345μH	199.9μH
L_o	232μH	311.29μH	232μH
C_o	16.6nF	9.1378nF	16.66nF
R_o	54Ω	52.4Ω	92Ω

Figure 3.3 shows the simulation results. In all cases, the simulation results using the new formulation matches perfectly with the exact solutions. The derivation is free of algebraic error!

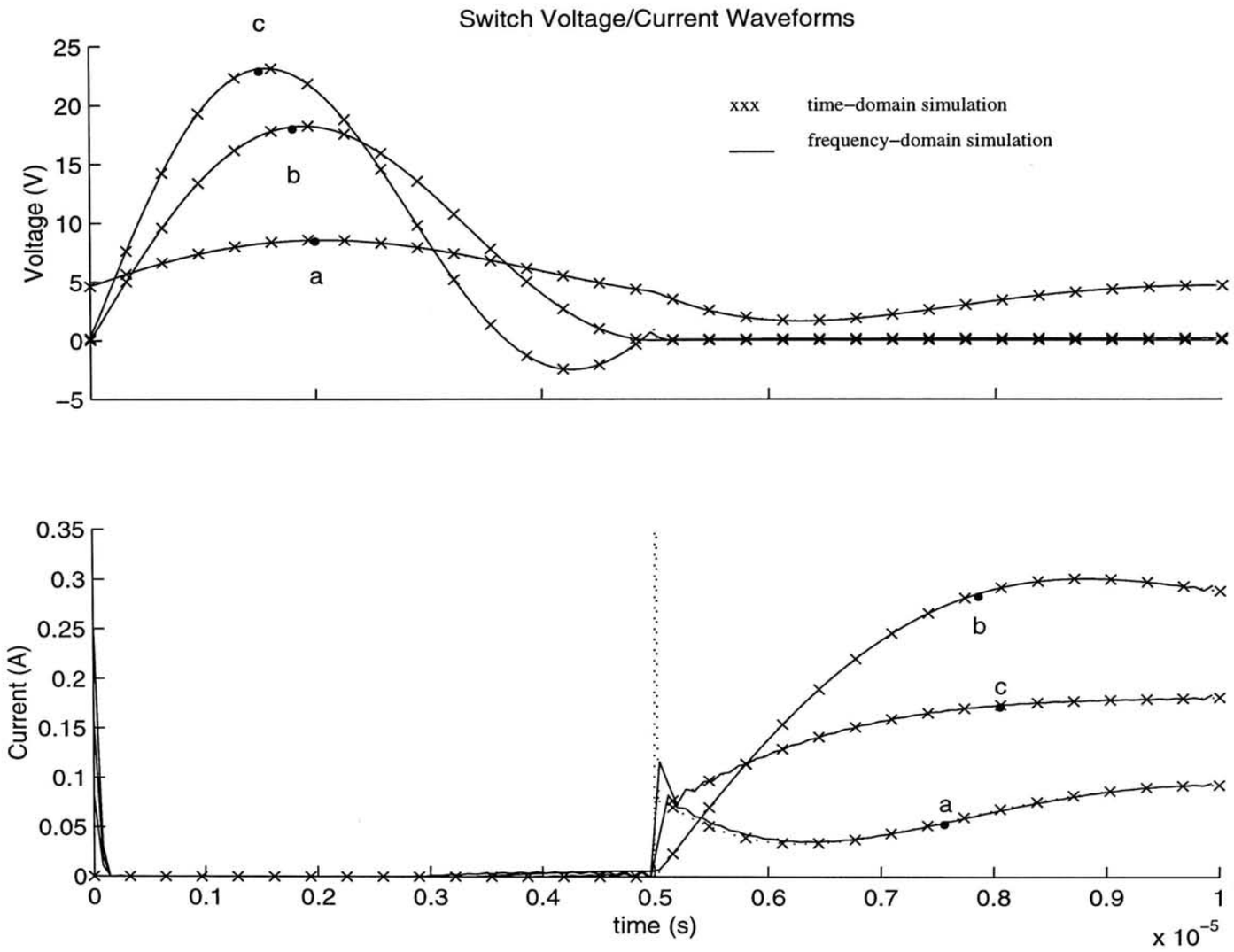


Figure 3.3 Simulated Waveforms using Time/Frequency Approaches

Even though the frequency domain approach requires larger computer resources in terms of CPU time and memory in comparison with the state-space approach, the state-space approach has difficulties in simulating microwave components that do not have simple time characteristics. Besides, the most powerful feature of the new formulation rests on its ability to synthesize load termination conditions to achieve Optimum Class-E conditions unobtainable through all other simulations.

3.3 Optimization

Previous section deals with the analysis of an arbitrary load network. This section will be devoted to the synthesis of load network to optimize the circuit performance. The objective is to achieve high efficiency given by:

$$\eta = \frac{P_n}{P_{dc}} \tag{3.17}$$

where P_n = Output Power at desired nth Harmonic
(n = 1 for amplifier)

P_{dc} = DC Power Consumption of the circuit

Optimum Class-E conditions of zero-voltage and zero-sloping avoids power dissipation across the active device, it does not eliminates harmonic dissipation.

The equation which gives the power delivered to a certain load at a particular frequency is given by:

$$P_k = \frac{1}{2} V_k I_k \cos(\phi) \tag{3.18}$$

where V_k , I_k = Voltage/Current Amplitude

ϕ = phase between Voltage/Current

Undesirable harmonic power dissipation can be suppressed by setting either their corresponding voltage/current amplitude to zero(non-coexistence) or put them in phase-quadrature(i.e., $\phi = 0$). Zero voltage/current can be achieved by short/open load terminations while phase-quadrature requires an imaginary load termination jX.

Principle of non-coexistence or phase-quadrature to harmonic suppression operates in pure frequency domain. On the other hand, Optimum Class-E conditions relate circuit performances in time domain. To corporate both desirable features offered by harmonic tuning and waveform shaping, Optimum Class-E conditions are re-expressed in frequency domain.

The optimization process is made possible by expressing the Optimum Class-E conditions in terms of the load network input port current components in frequency domain. DC biasing voltage V_{10} can also be related similarly. Principle of non-coexistence or phase-quadrature further constrains the current components. Under all these constrains, current vectors can be solved independent of any load network. The voltage vector then relates to the current vector through (3.12). Optimum Load terminations can be obtained by dividing corresponding voltage/current components. Optimum circuit performances can then be evaluated independent of any load network chosen for their realization. This allows the determination of the upper limits that can be achieved by a given active device without fixing a priori a topology[39].

3.3.1 Frequency Domain Class-E Definition

The first Optimum Class-E condition relates the turn-on voltage, $v_1(\theta_c)$.

Recall from (3.7b):

$$v_1(\theta_c) = -\frac{\left(1-e^{-\alpha}\right)R_{on} + \frac{\theta_c - \theta_o}{B}}{1-e^{-\alpha}} I_{10} + \frac{\sum_{\substack{m\neq 0 \\ m=-\infty}}^{\infty} \left\{ \frac{R_{on}}{1+jmBR_{on}} \left[e^{-\alpha + jm\theta_c} - e^{jm\theta_o} \right] - \frac{e^{jm\theta_c} - e^{jm\theta_o}}{jmB} \right\}}{1-e^{-\alpha}} I_{1m} \quad (3.19a)$$

The second Optimum Class-E relates the voltage time slope at turn-on, $\xi = \left.\frac{dv_1(\theta)}{d\theta}\right|_{\theta=\theta_c}$

Recall from (3.3c)

$$v_{1OFF}(\theta) = -\frac{\theta - \theta_o}{B} I_{10} - \sum_{\substack{m\neq 0 \\ m=-\infty}}^{\infty} \frac{e^{jm\theta} - e^{jm\theta_o}}{jmB} I_{1m} + v_1(\theta_o)$$

Denoting the time slope of the switch voltage at turn-on by ξ, one has

$$\xi = \left.\frac{dv_{1OFF}(\theta)}{d\theta}\right|_{\theta=\theta_c} = -\frac{1}{B} I_{10} - \sum_{\substack{m\neq 0 \\ m=-\infty}}^{\infty} \frac{e^{jm\theta_c}}{B} I_{1m} \quad (3.19b)$$

For general considerations, the turn-on voltage and its time-sloping will be left as design parameters and will not be set to zero.

The DC supply voltage is usually constrained by the system requirement. It is a pre-determined parameter. Recall from (3.11b),

$$2\pi V_{10} = -\left[\left(\frac{(\theta_c-\theta_o)^2}{B}\right)\left(\frac{1}{2}+\frac{e^{-\alpha}}{1-e^{-\alpha}}\right)+(2\pi+\theta_c-\theta_o)R_{on}\right]I_{10}$$

$$+\sum_{\substack{m\neq 0\\ m=-\infty}}^{\infty}\left[\frac{1}{m^2B}\left(e^{jm\theta_c}-e^{jm\theta_o}\right)-\frac{\theta_c-\theta_o}{jmB}\frac{1}{1+jmBR_{on}}\frac{1}{1-e^{-\alpha}}\left(e^{-\alpha+jm\theta_c}-e^{jm\theta_o}\right)\right]I_{1m} \quad (3.19c)$$

(3.19a-c) constrains the current vector by the voltage turn-on conditions and DC bias condition. By decomposing all complex variables into its real and imaginary parts (denoted by additional subscript "r" and "i" respectively), notice that $i_1(\theta)$ is real, negative frequency components are complex conjugate of their positive frequency counterparts, the summation boundary in (3.19a-c) can be reduced to include positive frequency components only. Consideration of up to M harmonic current components, (3.19a-c) can be expressed in matrix form given by:

$$\mathbf{U}\bar{\mathbf{I}} = \mathbf{H} \quad (3.20)$$

$$\bar{\mathbf{I}} = [I_{10} \quad I_{11r} \quad I_{11i} \quad I_{12r} \quad I_{12i} \quad \cdots \quad I_{1Mr} \quad I_{1Mi}]^T$$

where $\mathbf{U} = [U_{lm}]$ which is a 3x(2M+1) matrix

$\mathbf{H} = [H_{l1}]$ which is a 3x1 vector

and define

$$OP_m = \frac{R_{on}}{1+jmBR_{on}}\left[e^{-\alpha+jm\theta_c}-e^{jm\theta_o}\right]-\frac{e^{jm\theta_c}-e^{jm\theta_o}}{jmB} \quad (3.21a)$$

$$OQ_m = e^{jm\theta_c} \quad (3.21b)$$

$$D_m = \left[\frac{1}{m^2 B}\left(e^{jm\theta_c} - e^{jm\theta_o}\right) - \frac{\theta_c - \theta_o}{jmB} \frac{1}{1 + jmBR_{on}} \frac{1}{1 - e^{-\alpha}}\left(e^{-\alpha + jm\theta_c} - e^{jm\theta_o}\right) \right]$$

(3.21c)

Fill the matrix elements by:

$$\begin{aligned}
\mathbf{U}(1,1) &= -\frac{1}{2}\left[\left(1 - e^{-\alpha}\right) R_{on} + \frac{\theta_c - \theta_o}{B} \right] \\
\mathbf{U}(2,1) &= \frac{1}{2} \\
\mathbf{U}(3,1) &= -\frac{1}{2}\left[\frac{(\theta_c - \theta_o)^2}{B}\left(\frac{1}{2} + \frac{e^{-\alpha}}{1 - e^{-\alpha}}\right) + (2\pi + \theta_c - \theta_o) R_{on} \right]
\end{aligned} \qquad (3.21d)$$

$$\begin{aligned}
&\mathbf{U}(1,2m) = real\{OP_m\} \quad U(1,2m+1) = -imag\{OP_m\} \\
&\mathbf{U}(2,2m) = real\{OQ_m\} \quad U(2,2m+1) = -imag\{OQ_m\} \quad \{m = 1,2,3,\cdots M\} \\
&\mathbf{U}(3,2m) = real\{D_m\} \quad U(3,2m+1) = -imag\{D_m\}
\end{aligned} \qquad (3.21e)$$

$$\begin{aligned}
\mathbf{H}(1) &= \frac{1 - e^{-\alpha}}{2} v_1(\theta_c) \\
\mathbf{H}(2) &= -\frac{B}{2}\xi \\
\mathbf{H}(3) &= \pi V_{10}
\end{aligned} \qquad (3.21f)$$

H is the force term in (3.20) where the turn-on voltage, its time slope and DC bias are specified by the designer. (3.20) re-expresses the Class-E conditions and DC bias information in frequency domain. In case the force term **H** is filled with $v_1(\theta_c) = 0$ and $\xi = 0$, (3.20) specify the Optimum Class-E conditions in frequency domain. In short, (3.20) expresses the frequency domain definition of Class-E conditions.

3.3.2 Power Approach

In this approach, output power at harmonic frequencies (including fundamental frequency) is expressed as a quadratic function of the current vector. Output power at undesired harmonic frequencies are usually but not necessarily set to zero while output power at desired harmonic (fundamental for PA, 2nd harmonic for doubler) are set by system specifications. Optimum Class-E conditions specify in (3.20) already ensure minimum power dissipation across the active device, by setting all undesirable harmonic power to zero necessarily optimizing the power efficiency defined by (3.17). For radio transmitter application, harmonic power is usually suppressed to a minimum level say -- 40dBc. In case undesired harmonic levels are set to 0(though not required in this formulation), either principles of non-coexistence or phase-quadrature will be observed automatically through (3.18).

Recall from (3.11a),

$$V_{1n} = \sum_{m=1}^{\infty} S_{nm} I_{1m} + T_{nm} I_{1m}^{*} + (XI)_n I_{10} \tag{3.22}$$

Output power at nth harmonic P_n is given by:

$$P_n = 2real\{V_{1n} I_{1n}^{*}\} \tag{3.23}$$

Combine (3.22) and (3.23) and decomposing all variables into their real and imaginary part results:

$$\begin{aligned} \frac{P_n}{2} = \sum_{m=1}^{\infty} \quad & (S_{nmr} + T_{nmr}) I_{1mr} I_{1nr} + (T_{nmi} - S_{nmi}) I_{1mi} I_{1nr} + \\ & (S_{nmi} + T_{nmi}) I_{1mr} I_{1ni} + (S_{nmr} - T_{nmr}) I_{1mi} I_{1ni} + \\ & (XI)_{nr} I_{10} I_{1nr} + (XI)_{ni} I_{10} I_{1ni} \end{aligned} \tag{3.24}$$

(3.24) states that the harmonic power is a quadratic function of the current vector. When expressed in matrix form, for every harmonic, one has:

$$\frac{P_n}{2} = \{\mathbf{L}\bar{\mathbf{I}}\}^T \{\mathbf{R}_n \bar{\mathbf{I}}\} \tag{3.25}$$

$$\bar{\mathbf{I}} = [I_{10} \quad I_{11r} \quad I_{11i} \quad I_{12r} \quad I_{12i} \quad \cdots \quad I_{1Mr} \quad I_{1Mi}]^T$$

where $\mathbf{L} = [L]$ which is a 6x(2M+1) matrix

$\mathbf{R}_n = [H]$ which is a 6x(2M+1) matrix

and

$$\begin{aligned}
L(1,1) &= real\{(XI)_n\} & R_n(1,2n) &= 1 \\
L(2,1) &= imag\{(XI)_n\} & R_n(2,2n+1) &= 1 \\
L(3,2m) &= real\{S_{nm}\} + real\{T_{nm}\} & R_n(3,2n) &= 1 \\
L(4,2m+1) &= -imag\{S_{nm}\} + imag\{T_{nm}\} & R_n(4,2n+1) &= 1 \\
L(5,2m) &= imag\{S_{nm}\} + imag\{T_{nm}\} & R_n(5,2n) &= 1 \\
L(6,2m+1) &= real\{S_{nm}\} - real\{T_{nm}\} & R_n(6,2n+1) &= 1
\end{aligned}$$

{where m = 1,2,3⋯,M} {where n = harmonic index}

{unfilled elements are set to 0} {unfilled elements are set to 0}

(3.26)

Note that the power equation (3.25) is set independent of the Class-E definition equation (3.20). To incorporate Class-E conditions in the power equation, (3.20) must be reformulated.

De-compose **U** in (3.20) into $\mathbf{U_L}$ and $\mathbf{U_R}$:

$$\overbrace{\begin{bmatrix} \mathbf{U}(1,1) & \mathbf{U}(1,2) & \mathbf{U}(1,3) & \mathbf{U}(1,4) & \mathbf{U}(1,5) & \mathbf{U}(1,6) & \bullet & \bullet & \mathbf{U}(1,2M+1) \\ \mathbf{U}(2,1) & \mathbf{U}(2,2) & \mathbf{U}(2,3) & \mathbf{U}(2,4) & \bullet & \bullet & \bullet & \bullet & \mathbf{U}(2,2M+1) \\ \mathbf{U}(3,1) & \mathbf{U}(3,2) & \mathbf{U}(3,3) & \mathbf{U}(3,4) & \bullet & \bullet & \bullet & \bullet & \mathbf{U}(3,2M+1) \end{bmatrix}}^{[\mathbf{U}]_{3\times(2M+1)}} \overbrace{\begin{bmatrix} I_{10} \\ I_{11r} \\ I_{11i} \\ I_{12r} \\ I_{12i} \\ \bullet \\ \bullet \\ \bullet \\ I_{1Mr} \\ I_{1Mi} \end{bmatrix}}^{[\bar{\mathbf{I}}]_{(2M+1)\times 1}} = \overbrace{\begin{bmatrix} \mathbf{H}(1) \\ \mathbf{H}(2) \\ \mathbf{H}(3) \end{bmatrix}}^{[\mathbf{H}]_{3\times 1}}$$

$[\mathbf{U}_{\mathbf{L}}]_{3\times 3}$ $[\mathbf{U}_{\mathbf{R}}]_{3\times(2M-2)}$

(3.27)

(3.27) constitutes an underdetermined system, 2M+1 unknown current components but with 3 equations. Three current components can be eliminated. Solution to (3.27) can be expressed as:

$$\overbrace{\begin{bmatrix} I_{10} \\ I_{11r} \\ I_{11i} \\ \hline I_{12r} \\ I_{12i} \\ \bullet \\ \bullet \\ \bullet \\ I_{1Mr} \\ I_{1Mi} \end{bmatrix}}^{[\bar{\mathbf{I}}]_{2M+1)\times 1}} = \overbrace{\left[\begin{array}{cc} -\mathbf{U}_{\mathbf{L}}^{-1}\mathbf{U}_{\mathbf{R}} & \mathbf{U}_{\mathbf{L}}^{-1}\mathbf{H} \\ \hline & \\ [\mathbf{id}]_{(2M-2)(2M-2)} & [\mathbf{0}]_{(2M-2)\times 1} \\ & \end{array}\right]}^{[\mathbf{E}]_{(2M+1)(2M-1)}} \overbrace{\begin{bmatrix} I_{12r} \\ I_{12i} \\ I_{13r} \\ I_{13i} \\ \bullet \\ \bullet \\ \bullet \\ I_{1Mr} \\ I_{1Mi} \\ \hline 1 \end{bmatrix}}^{[\bar{\mathbf{I}}]_{2M-1)\times 1}}$$

(3.28)

where $\mathbf{id}$ = (2M-2) × (2M-2) identity matrix

$\mathbf{0}$ = (2M-2) ×1 zero matrix

(3.28) relates the complete current vector $\bar{\mathbf{I}}$ to the reduced current vector $\tilde{\mathbf{I}}$ through **E**. i.e., $\bar{\mathbf{I}} = \mathbf{E}\tilde{\mathbf{I}}$. Substituting (3.28) into (3.25), we get

$$\frac{P_n}{2} = \tilde{\mathbf{I}}^T \mathbf{C}_n \tilde{\mathbf{I}} \tag{3.29a}$$

$$\text{where } \mathbf{C}_n = \mathbf{E}^T \mathbf{L}^T \mathbf{R}_n \mathbf{E} \tag{3.29b}$$

Consider M harmonic currents, there are 2M+1 unknowns (real and imaginary parts of harmonic current components + DC component). Optimum Class-E and DC-bias conditions eliminate 3 unknowns. 2M-2 unknowns are left to be solved. On the other hand, there are M non-linear power equations specifying the harmonic power spectrum.

$$\mathbf{F} = \begin{bmatrix} P_1 \\ P_2 \\ \cdot \\ \cdot \\ \cdot \\ P_M \end{bmatrix} - \begin{bmatrix} \tilde{\mathbf{I}}^T \mathbf{C}_1 \tilde{\mathbf{I}} \\ \tilde{\mathbf{I}}^T \mathbf{C}_2 \tilde{\mathbf{I}} \\ \\ \\ \\ \tilde{\mathbf{I}}^T \mathbf{C}_M \tilde{\mathbf{I}} \end{bmatrix} \tag{3.30a}$$

The optimization problem becomes that of finding the reduced current vector $\tilde{\mathbf{I}}$ which evaluates **F** to zero. This can be achieved through various efficient gradient search algorithms. The exact gradient of (3.30a) is given below:

$$\begin{aligned} \frac{\partial \mathbf{F}^T}{\partial \tilde{\mathbf{I}}} &= \left[\frac{\partial \mathbf{F}_1}{\partial \tilde{\mathbf{I}}} \quad \frac{\partial \mathbf{F}_2}{\partial \tilde{\mathbf{I}}} \quad \cdots \quad \frac{\partial \mathbf{F}_M}{\partial \tilde{\mathbf{I}}} \right] \\ &= \left[\left(\mathbf{C}_1 + \mathbf{C}_1^T\right)\tilde{\mathbf{I}} \quad \left(\mathbf{C}_2 + \mathbf{C}_2^T\right)\tilde{\mathbf{I}} \quad \cdots \quad \left(\mathbf{C}_M + \mathbf{C}_M^T\right)\tilde{\mathbf{I}} \right] \end{aligned} \tag{3.30b}$$

Note that the last element in $\tilde{\mathbf{I}}$ is a constant 1.

Since multiple solutions exists a good initial guess ensures a reasonable solution with fast convergence. Under all circumstances, any solution should be checked against device maximum ratings or existence of excessive negative voltage/current.

For M=2 case, analytical solution for R_{on}=0 under 50% duty ratio with zero harmonic dissipation has been derived and given below:

$$\begin{cases} I_{11r} = \beta I_{10} \\ I_{11i} = \dfrac{\pi}{4} I_{10} \\ I_{12r} = \left(\beta - \dfrac{1}{2}\right) I_{10} \\ I_{12i} = 2BV_{10} + \dfrac{4}{\pi}\beta I_{10} \end{cases} \qquad \textit{where} \quad \beta = \sqrt{-\frac{\pi B}{4}\frac{V_{10}}{I_{10}}}, \quad I_{10} = -\frac{P_1}{V_{10}} \tag{3.31}$$

(3.31) serves a very good initial guess for the 2-harmonic case.

Once the reduced current vector $\tilde{\mathbf{I}}$ has been solved, the complete current vector $\bar{I}$ can be obtained through (3.28). The voltage responses are obtained through (3.12). Optimum load terminations can be evaluated by dividing the corresponding voltage/current components. System performance merit can be evaluated accordingly.

To summarize, the optimization procedure derived in this sub-section can be used to optimize the load termination conditions under user specified harmonic power spectrum. The steps are outlined below:

1. Given dc voltage bias V_{10} , Class-E conditions $v_1(\theta_c)$ and ξ (optimally both set to zero) , switch-capacitor parameters R_{on} and C_{out}.

2. Set the required harmonic power spectrum.

3. Solve the reduced current vector $\tilde{\mathbf{I}}$ in (3.30a) with the help of the gradient information provided by (3.30b). For 2-harmonic case, (3.31) serves as a good initial solution.

4. Obtain the complete current vector $\bar{I}$ by (3.28) and voltage responses by (3.12).

5. Evaluate other derived quantities such as optimum load terminations, efficiency and device stresses.

3.3.3 Harmonic Reactance Approach

The power approach described in previous sub-section is very useful for that designer can specify the complete harmonic power spectrum. Solution to (3.30a) requires iterative numerical searching. Even equipped with the powerful gradient information, the searching algorithms may still diverge if the initial guess is far from the desired solution. The 2 harmonic case is fortunate enough to have analytical solution under simplified conditions to serve as an initial guess. It cannot be generalized to higher harmonic cases. In these cases, the powerful feature to specify harmonic spectrum is sacrificed for ease of implementation. In contrast to the power approach, harmonic terminations are specified in this approach. Harmonic voltages are expressed in terms of the harmonic terminations and the harmonic currents. This together with the Class-E conditions specified in (3.20) is sufficient to solve the unknown current vector. System performance can then be evaluated accordingly.

Again, recall from (3.11a),

$$V_{1n} = \sum_{m=1}^{\infty} S_{nm} I_{1m} + T_{nm} I_{1m}^{*} + (XI)_n I_{10} \tag{3.32}$$

To suppress undesired nth harmonic power, the principle of non-coexistence or phase-quadrature requires the Class-E load network input port load impedance Z_{1n} at harmonic n be purely imaginary, i.e.

$$\begin{aligned} & Z_{1n} = jX_n \\ \Rightarrow \quad & V_{1n} = jX_n I_{1n} \end{aligned} \tag{3.33}$$

Combining (3.32) and (3.33) and equating the real and imaginary parts results in two additional linear equations in terms of the current components:

$$\begin{aligned} (XI)_{nr} I_{10} + \sum_{m=1}^{\infty} [(S_{nmr} + T_{nmr}) I_{1mr} + (-S_{nmi} + T_{nmi}) I_{1mi}] + X_n I_{1ni} = 0 \\ (XI)_{ni} I_{10} + \sum_{m=1}^{\infty} [(S_{nmi} + T_{nmi}) I_{1mr} + (S_{nmr} - T_{nmr}) I_{1mi}] - X_n I_{1nr} = 0 \end{aligned} \tag{3.34}$$

When coupled with the Class-E conditions specified by (3.20), the set of linear equations sufficiently determine the current vector.

Consider M non-zero harmonic currents, number of unknowns is 2M+1 (real and imaginary part + DC current components). On the other hand, for each additional harmonic considered, (3.34) generates 2 additional equations. Therefore, there are 2(M-1) linear equations. The Class-E conditions in (3.20) specify 3 more equations. The system of linear equations is sufficiently determined because number of unknowns is equal to the number of independent equations.

For given harmonic reactances at undesired harmonics, the current components can be solved through the system of linear equations defined by (3.20) and (3.34). Voltage components are obtainable through (3.12). Optimum load terminations can be evaluated by dividing the corresponding harmonic voltage /current components. Other derived quantities such as output power and efficiency can be easily calculated. Like the usual practice, maximum device stresses and other time domain constrains such as the negative voltage/current for a particular device should be observed.

The harmonic reactance approach to circuit optimization has the added advantage of easy implementation and a unique solution. The down-side of this approach is that the output power is not fully controllable.

The two approaches can be combined by sweeping the harmonic reactance and noting the output power. When the output power is sufficiently close to the required level, the solutions generated by the harmonic approach can be used as the initial solution for the power approach. The combined approach ensures a good convergence while being able to meet the system requirement such as the output power level.

3.4 Summary

A novel analysis method based on the harmonic balance technique has been developed and verified. The new formulation is capable of analyzing circuit performances with arbitrary load terminations, independent of their topology of implementation.

Optimum Class-E conditions were re-expressed in frequency domain. Ideas of waveform shaping and harmonic tuning were therefore combined under the framework of frequency domain.

The structure of the new formulation was further exploited to optimize the circuit performances. Two different approaches were proposed:

The Power Approach is capable of synthesizing optimum load terminations to meet the output power requirements. Iterative searching algorithms assisted by exact gradient information are employed to solve the system of quadratic power equations. For 2-harmonic case, analytical solution for the lossless Class-E serves as a good initial solution to assist convergence. For general harmonic cases, convergence is the major concern.

The Harmonic Reactance Approach avoids harmonic dissipation by explicitly specifying the load terminations at undesired harmonics to be purely imaginary. When coupled with the Class-E conditions, the system of linear equations relating the harmonic current components is sufficiently determined. Other derived

quantities such as the output power, efficiency, optimum load termination at the desired frequency can be uniquely determined. The Harmonic Reactance Approach suffers from its inability to control output power level.

The advantages of both methods can be combined in a hybrid approach. The Harmonic Reactance Approach sweeps the harmonic reactances in search of possible solutions satisfying the output power requirement. The solution is then used as initial guess for further refinement by the Power Approach.

Under all cases, maximum device stresses and other time domain constrains such as the excessive negative voltage/current should be observed.

Chapter 4 Performance Evaluations

Previous chapter details the theoretical development of analysis and synthesis of Class-E circuit in frequency domain. Because of the existence of unavoidable tolerance in circuit fabrication, over-simplified assumptions made on theoretical development, power amplifiers which possess good performance and robustness may not be realized by the idealized optimum design.

The purpose of this chapter is to study the effects of circuit variations on the performance of Class-E power amplifier. This is made possible with extensive application of the general analysis and synthesis capabilities inherent in the new formulation.

Effects such as the non-zero turn-on resistance, frequency variations, load variations, harmonic terminations and packaging that are of primary interest to circuit designers will be investigated thoroughly. Other aspects such as the voltage and its time slope at turn on will be too abstract from designers' point of view and will not be studied explicitly in this chapter. Duty ratio of 50% is assured throughout the study for it is most economical to achieve at microwave frequencies.

4.1 Benchmarks

Before a detailed investigation, some benchmarks must be established for normalization. Obviously one such common reference is the conventional Class-E with zero turn-on resistance. For consistence with our nomenclature, the operation of the lossless Class-E will be re-established. Key functional characteristics will be set as common references.

The derivation of the lossless Class-E follows a similar but simpler procedure described in the previous chapter. The governing equations in frequency domain are given by:

$$V_{10} = -\frac{1}{2\pi B}\left\{\frac{1}{2}(\theta_c-\theta_o)^2 I_{10} - \sum_{\substack{m\neq 0\\ m=-\infty}}^{\infty} \frac{e^{jm\theta_c}-e^{jm\theta_o}}{m^2} I_{1m} + j(\theta_c-\theta_o)\sum_{\substack{m\neq 0\\ m=-\infty}}^{\infty} \frac{e^{jm\theta_o}}{m} I_{1m}\right\} \quad (4.1)$$

$$V_{1n} = -\frac{1}{2\pi B}\left\{\begin{array}{l}\left[\dfrac{e^{-jn\theta_c}-e^{-jn\theta_0}}{n^2} - \dfrac{\theta_c-\theta_o}{jn}e^{-jn\theta_c}\right] I_{10} + \\ \left[-\dfrac{e^{-jn(\theta_c-\theta_0)}-1}{n^2} + \dfrac{\theta_c-\theta_o}{jn}\right] I_{1n} - \dfrac{\left(e^{-jn\theta_c}-e^{-jn\theta_o}\right)^2}{2n^2} I_{1n}^* - \\ \sum\limits_{\substack{m\neq 0\\ m\neq\pm n\\ m=-\infty}}^{\infty} \dfrac{e^{j(m-n)\theta_c}-e^{j(m-n)\theta_o}}{m(m-n)} I_{1m} - \left(e^{-jn\theta_c}-e^{-jn\theta_o}\right)\sum\limits_{\substack{m\neq 0\\ m\neq\pm n\\ m=-\infty}}^{\infty} \dfrac{e^{jm\theta_o}}{mn} I_{1m}\end{array}\right\} \quad (4.2)$$

The optimum Class-E conditions of zero voltage and zero-sloping conditions are given by:

$$I_{10} = \frac{j}{\theta_c-\theta_o}\sum_{\substack{m\neq 0\\ m=-\infty}}^{\infty} \frac{e^{jm\theta_c}-e^{jm\theta_o}}{m} I_{1m} \quad (4.3a)$$

$$I_{10} = -\sum_{\substack{m\neq 0\\ m=\infty}}^{\infty} e^{jm\theta_c} I_{1m} \quad (4.3b)$$

For single tone output current case under 50% duty ratio, solution to (4.3a) and (4.3b) exists for n=odd only. This means that frequency doubler is not possible under 50% duty ratio. For amplifer case (n=1), the following results can be obtained through (4.1)-(4.3):

$$Z_{10} = \frac{V_{10}}{I_{10}} = -\frac{1}{\pi B} \quad (4.4a)$$

$$Z_{11} = \frac{V_{11}}{I_{11}} = \frac{1}{2\pi B}\left[j2\pi + (4 + j\pi)e^{-j2\tan^{-1}\frac{\pi}{2}} \right] \tag{4.4b}$$

Because of 100% efficiency, (4.4a) implies:

$$P_1 = \pi B V_{10}^2 \tag{4.5}$$

(4.5) is similar to $P_{diss} = \frac{1}{2} fCV^2$ which describes the power dissipation associated with discharging a capacitor C with voltage V at frequency f. Optimum Class-E conditions require the complete discharge of C_{out} to the load before turn on, rf power is completely transferred to the load. In this sense, C_{out} functions as the power house where output power originates from. For a given voltage bias, the maximum operating frequency to achieve optimum Class-E is mainly limited by the device's current generating capabilities to discharge C_{out} completely before turn on.

(4.4b) further indicates that the optimum fundamental load impedance is normalized to C_{out} through $B = \omega C_{out}$. In contrast to all other classes of power amplifier, the optimum load is independent of the DC voltage bias. In microwave applications, C_{out} is necessarily the parasitic output capacitor intrinsic to power transistors. Once C_{out} is fixed, output power, optimum load impedance and maximum operating frequency are pre-determined.

For convenience in the subsequent discussions, normalization to DC bias voltage $V_{10} = 1$ and $B = \omega C_{out} = 1$ will be assumed throughout the chapter unless otherwise specified. The output power is also normalized to (4.5) by defining

$$P_1(dBe) = 10\log\frac{P_1}{\pi B V_{10}^2} \tag{4.6}$$

where P_1 = actual output power in general cases

For clarity, all normalized parameters will be underlined throughout the chapter.

4.2 Non-Zero Turn-on Resistance Variations

While C_{out} functions as the virtual power house, $\underline{R}_{on}$ is the major power dissipator, especially for low voltage supply applications. The resultant effects on the output power and efficiency are shown in Figure 4.1. It is apparent that the optimum load to achieve Optimum Class-E conditions of zero voltage and zero-sloping is a function of $\underline{R}_{on}$. Figure 4.2 shows the variation of the optimum load normalized to the reactance of the output capacitor, i.e. $\frac{1}{B}$. As normalized $\underline{R}_{on}$ increases from 0 to 0.3356, the optimum load, $\underline{Z}_{opt}$ moves from its values predicted by (4.4b) towards the rim of the Smith Chart. For $\underline{R}_{on}$ greater than 0.3356, all input power will be dissipated on the turn-on resistor if Optimum Class-E conditions are to be observed.

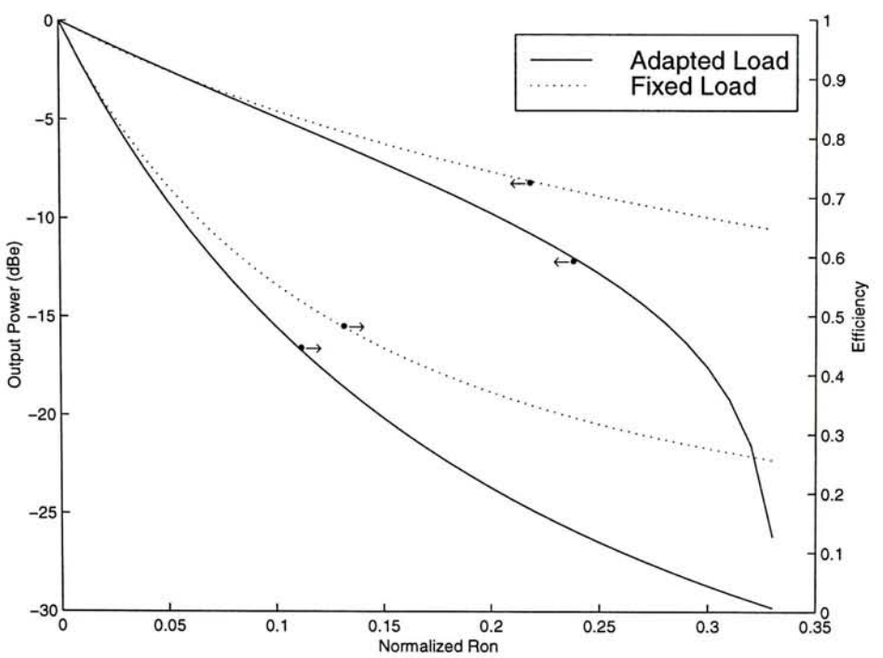


Figure 4.1 Efficiency and output power as a function of Normalized $\underline{R}$on

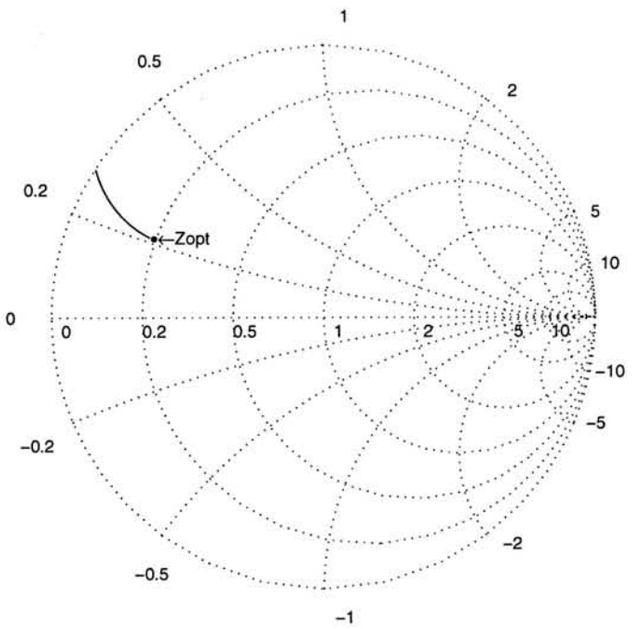


Figure 4.2 Normalized Optimum Class-E Load

It is interesting to note that the degradation of the output power and efficiency due to $\underline{R}_{on}$ is less profound with the load fixed by the value given in (4.4b). This implies that under large $\underline{R}_{on}$, Optimum Class-E conditions are not necessarily to be observed for optimum efficiency and power. However, $\underline{R}_{on}$ is in general less than 0.05 for most microwave power transistors and the two cases shown in Figure 4.1 are almost undifferentiable.

Figure 4.3 shows various voltage/current waveforms under different conditions. The solid lines on the left are voltage waveforms while the dashed lines represent their corresponding current waveforms. Case (1) denotes the lossless situation with $\underline{R}_{on}$ =0. Case(2) and case(3) show the switch waveforms for $\underline{R}_{on}$ =0.15. The voltage waveform in case(2) has been brought to zero voltage and zero-sloping with adapted optimum load. The corresponding switch current rises smoothly. Case(2) is more lossy due to a larger current which flows with larger i^2R loss in compare with case(3). In case(3), the load is

fixed by the value given in (4.4b). A large current spike results because Optimum Class-E conditions are no longer observed. This can be detrimental to the long term reliability of microwave transistors.

Under all cases, both output power and efficiency are severely degraded by non-zero $\underline{R}_{on}$.

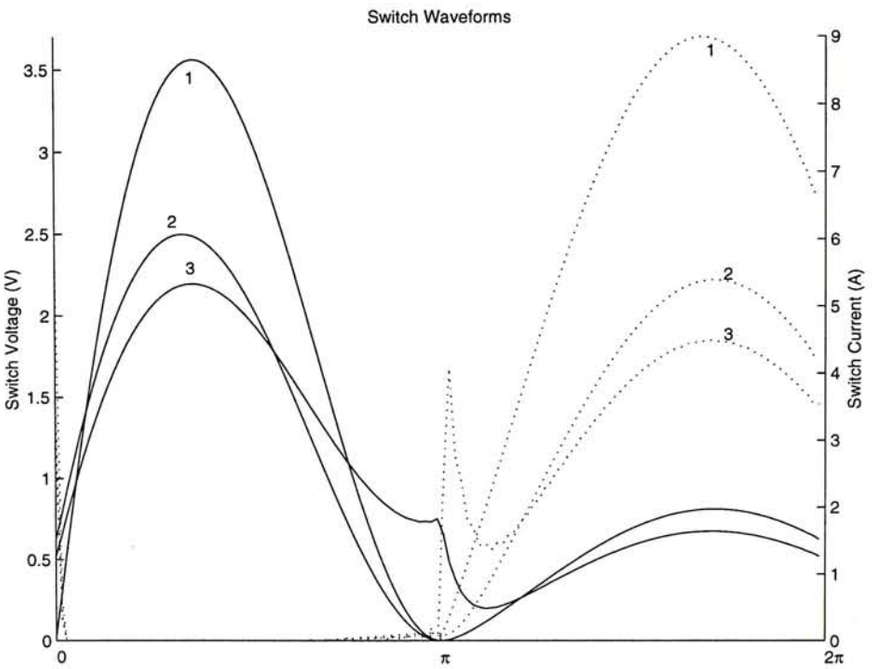


Figure 4.3 Voltage/current waveforms with different loading conditions

(1) $\underline{R}_{on}$=0; Load given by (4.4b)
(2) $\underline{R}_{on}$=0.15; Optimum Class-E Load
(3)$\underline{R}_{on}$=0.15; Load given by (4.4b)

4.3 Frequency Variation

The usable bandwidth is another important figure of merit to optimize in power amplifier design. Zero-sloping in Optimum Class-E condition permits accidental timing mistakes by ensuring zero voltage in a small time neighborhood at turn-on. The timing error can be caused by faster/slower switching frequency. Therefore, Class-E power amplifier is broadband in nature. Figure 4.4 shows the effects of frequency variations on the output power and efficiency. Amplifier efficiency remains relatively high over a bandwidth of almost an octave. The output power suffers a moderate decrease as frequency increases.

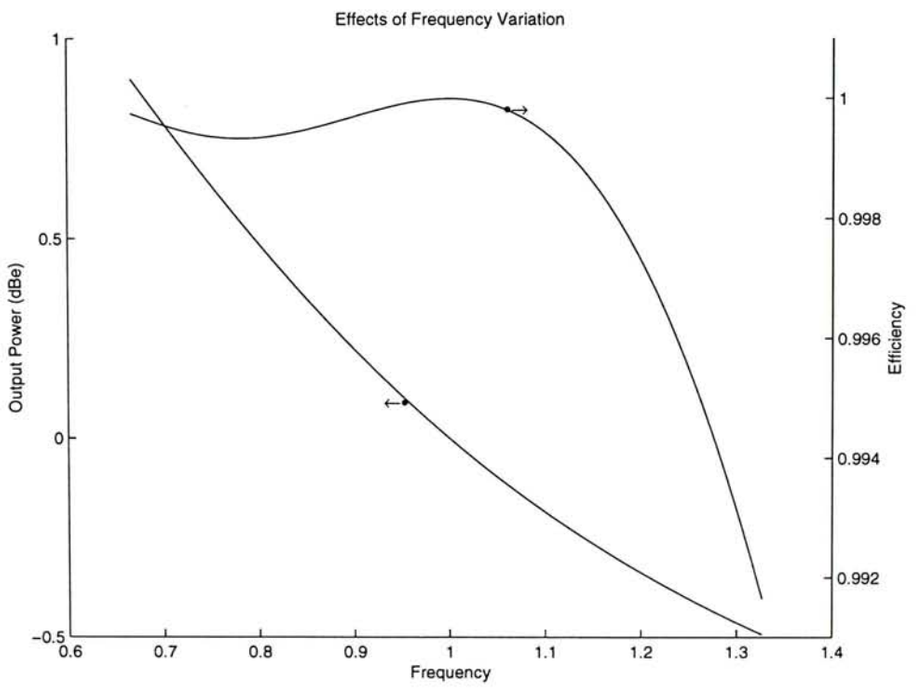


Figure 4.4 Output power and efficiency versus normalized frequency

The output power variations can be compensated with 2nd harmonic tuning. Figure 4.5 shows both optimum fundamental load and 2nd harmonic termination necessary to achieve an ultra flat output power response of 0 dBe. In the figure, the 2nd harmonic termination is kept at purely reflective so as not to create power losses. The fundamental load is relatively inert to frequency variations. This implies that as long as the 2nd harmonic termination is kept close to open circuit, broadband power efficient Class-E amplification is possible with a load that exhibits a flat amplitude and phase responses. In conventional series tuned Class-E configuration, the amplitude and phase responses of the fundamental load is limited by the high Q resonator. At microwave frequencies, the operating bandwidth of Class-E PA can be broadened by independent control of the fundamental load and higher harmonic terminations.

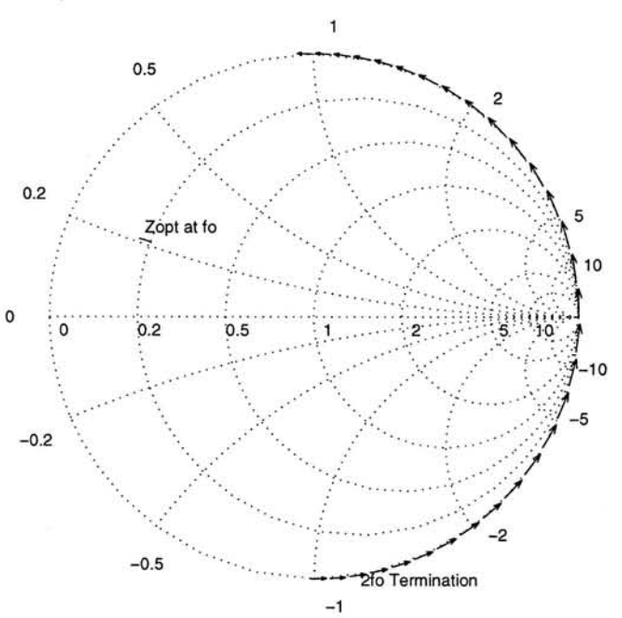


Figure 4.5 Optimum Load for Broadband Class-E PA

4.4 Fundamental Load Variations

Power amplifier design will not be possible if the optimum load exists only as a single spot on the impedance plane. Due to unavoidable uncertainties inherent in microwave circuit fabrication, a knowledge of the grace region is far more important than an ideal abstraction of the optimum point. Rate of performance degradation in the neighborhood of the optimum point dictates the relative ease of circuit implementation and its tolerance to parameter uncertainties as well.

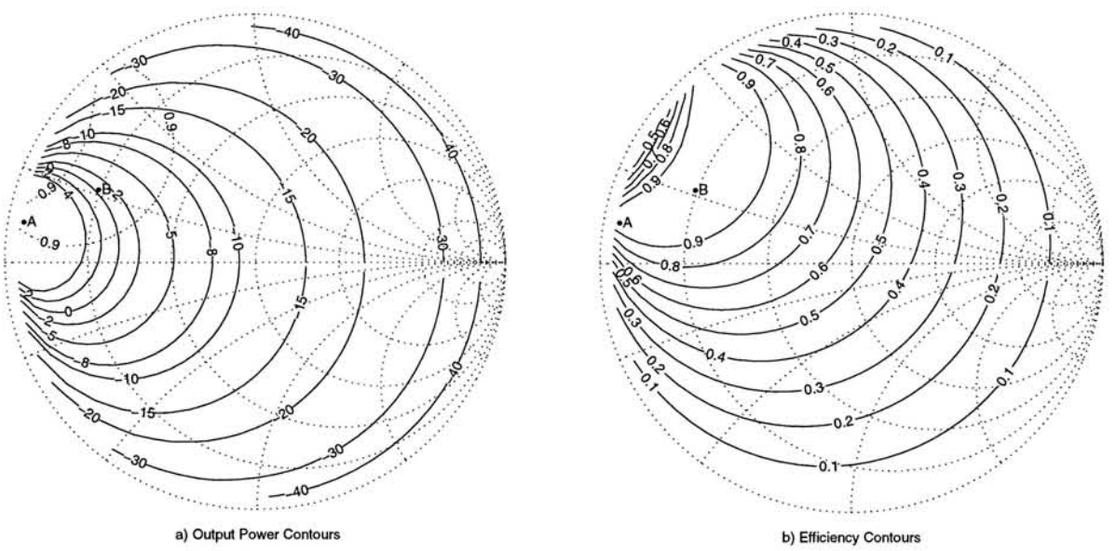


Figure 4.6 Output power(dBe) / efficiency contours of ideal Class-E PA
(Point A---optimum power; Point B---optimum efficiency)

Figure 4.6 shows the output power/efficiency contours of the Class-E PA on the Smith Charts normalized to the reactance of the transistor's output capacitor. Point A/B denote the optimum power point and optimum efficiency point respectively. It is apparent that

the two do not coincide. Point A is within the 4dBe power contour while point B rests on the 0 dBe line. Ultra high efficiency can be achieved at a cost of roughly 4dB output power. The 90% efficiency contour is superimposed on the power contour. It is apparent that high efficiency can be achieved within a relatively large grace region. However, within the grace region, output power varies significantly. The goal is to achieve high output power by moving from point B towards point A while still within the efficiency objectives.

The results shown in Figure 4.6 are somewhat too optimistic. The only loss mechanism accounted for is the $1/2\,fCV^2$ loss associated with discharging the finite output capacitor. The performance contour can be refined to include the finite turn-on resistor $\underline{R}_{on}$.

The Series of graphs in Figure 4.7 shows the effects of $\underline{R}_{on}$ on output power and efficiency contours. As $\underline{R}_{on}$ increases, both the optimum power point A and optimum efficiency point B relocate. Points A/B move further apart as a results of the increase of $\underline{R}_{on}$. This makes it more difficult to achieve simultaneous high efficiency and good output power level. The situation is further aggravated by the simultaneous shrinking of the grace region surrounding points A and B. For $\underline{R}_{on}$=0.01, 0 dBe output power level with 90% efficiency can be marginally achieved while $\underline{R}_{on}$ =0.02 achieve the same power level at 80% efficiency. Figure 4.7 III indicates that 80% efficiency can be achieved for a maximum power of -3dBe. The situation for $\underline{R}_{on}$ =0.04 gets worse, only -4dBe power can be achieved at 70% efficiency.

The existence of non-zero R_{on} not only alters the optimum design as revealed in section

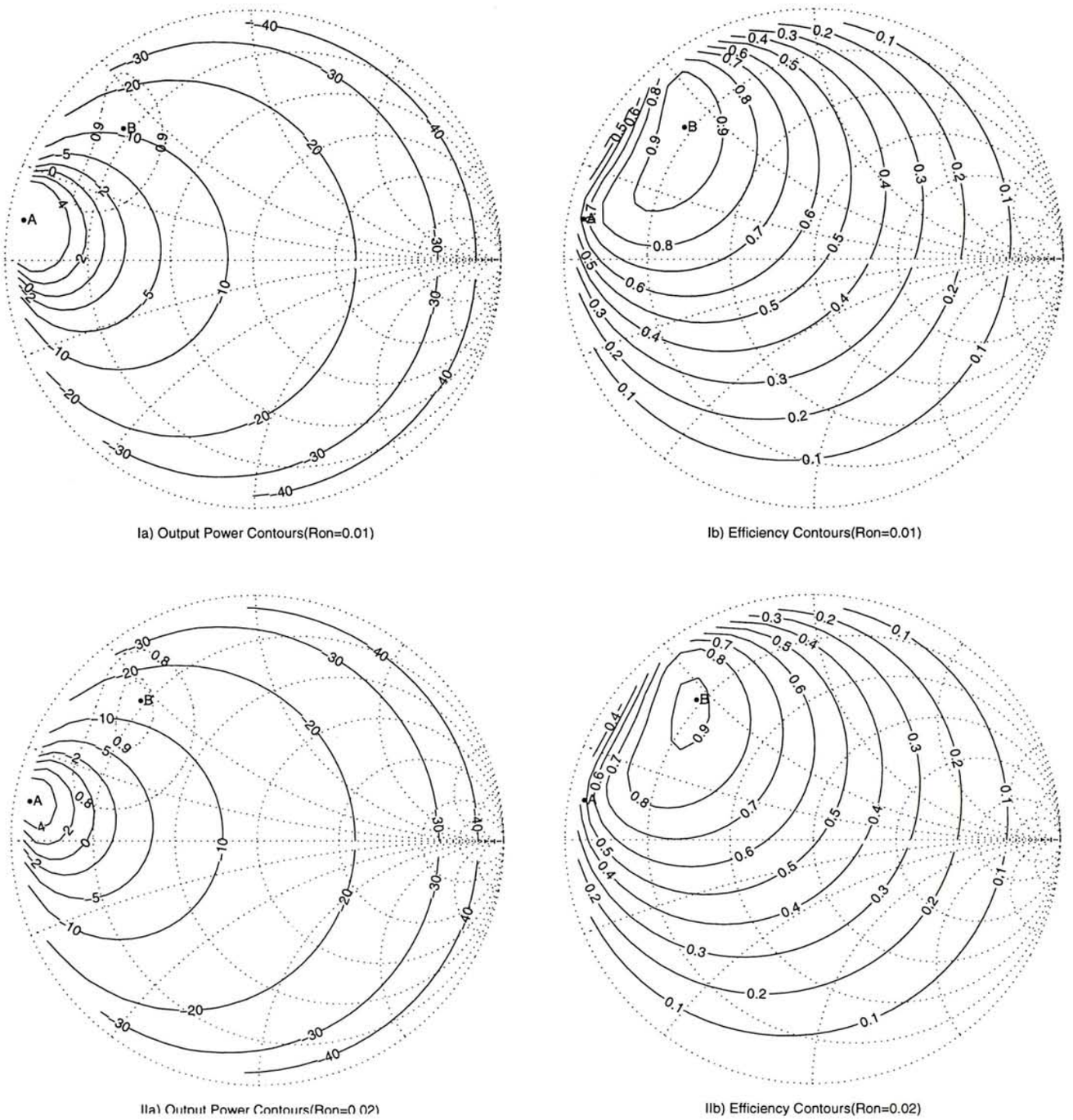
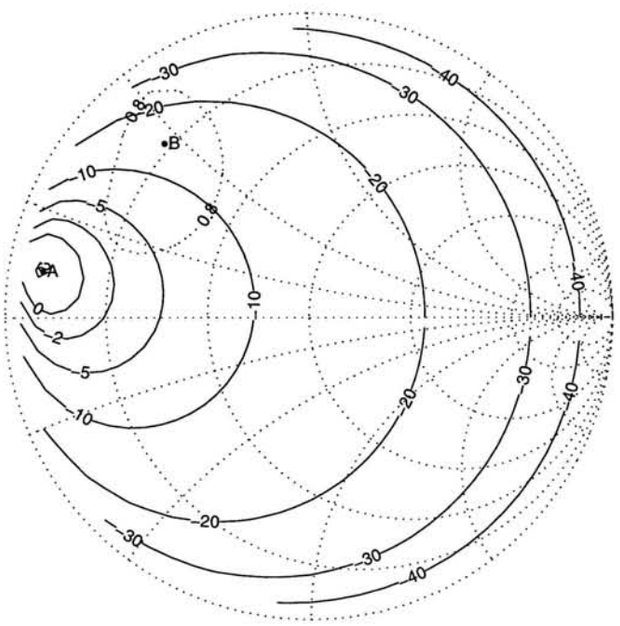
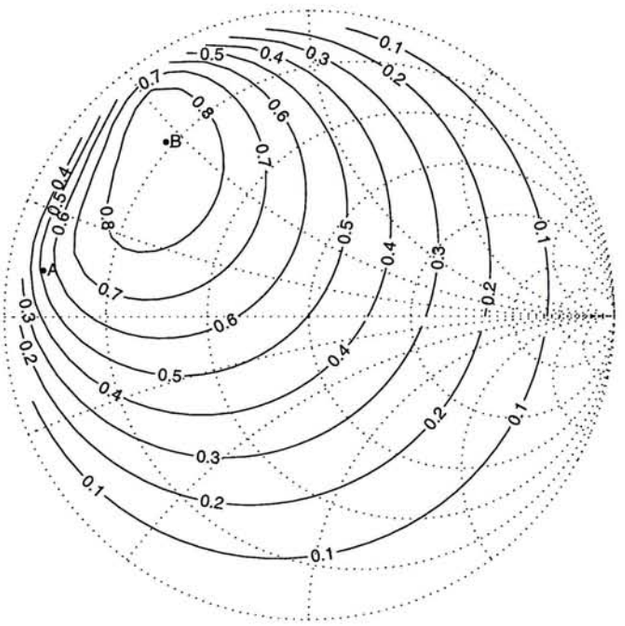


Figure 4.7 ***Output power(dBe) / efficiency contours as a function of*** $\underline{R}$***on***

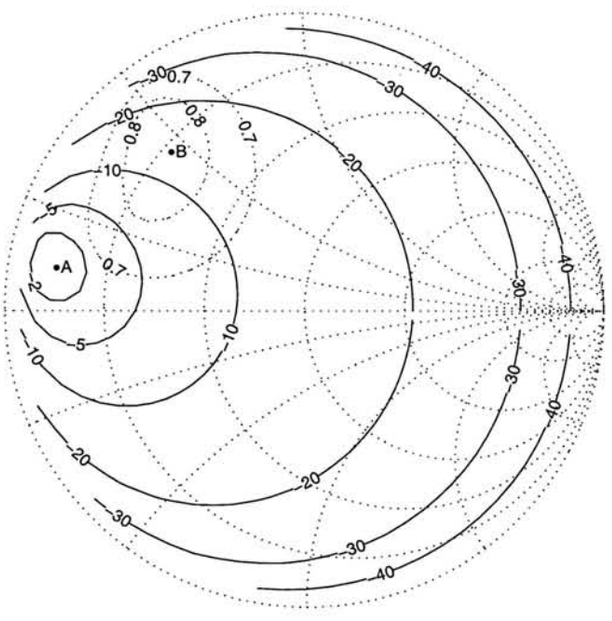
4.2 but also has a severe impact on both output power and achievable efficiency in general. The inclusion of $\underline{R}_{on}$ is crucial to the prediction of Class-E performance.



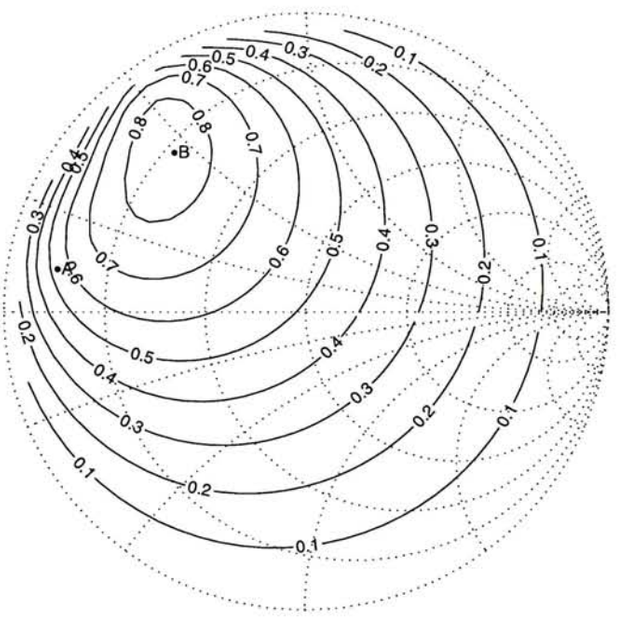
IIIa) Output Power Contours(Ron=0.03)



IIIb) Efficiency Contours(Ron=0.03)



IVa) Output Power Contours(Ron=0.04)



IVb) Efficiency Contours(Ron=0.04)

'Figure 4.7 Output power(dBe) / efficiency contours as a function of Ron

4.5 Harmonic Loading Variations

Conventional Class-E power amplifier assumes open circuit terminations for all harmonic frequencies. Practical implementation of open circuit over 3 harmonics at microwave frequencies is a non-trivial task[40]. Parasitics such as package effects and microstrip junction effects may offset the open circuit presented to the intrinsic transistor.

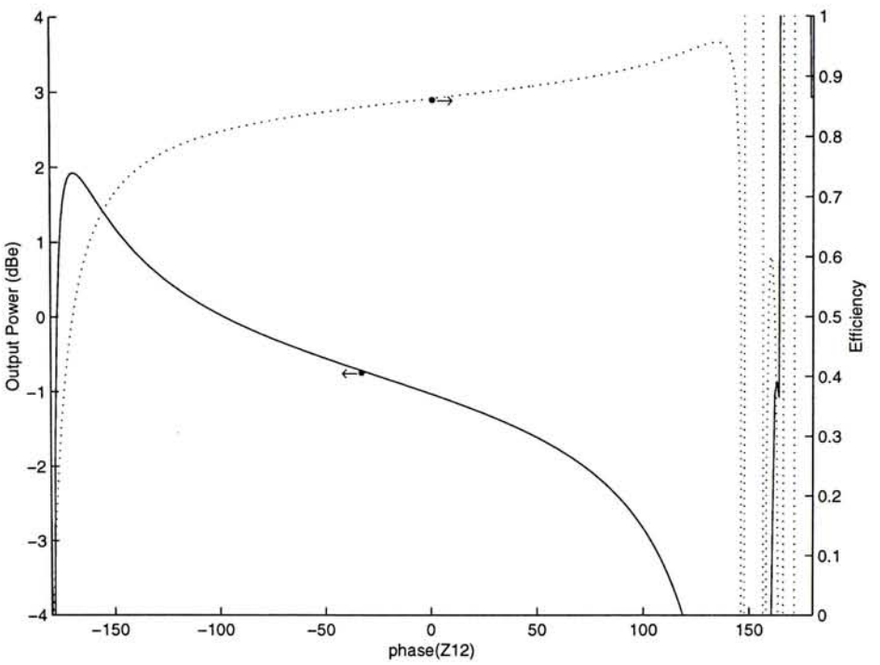


Figure 4.8 Output power(dBe) and efficiency as a function of 2nd harmonic termination($\underline{R}_{on}$=0.02)

Fortunately, optimum Class-E conditions may still be achieved under various harmonic terminations. Figure 4.8 shows the effects of 2nd harmonic loading on the Optimum Class-E PA performance. Figure 4.9 shows the relative harmonic voltage/current structure as a function of the phase of the 2nd harmonic reflection coefficient.

$\underline{R}_{on}$ =0.02 is assumed to show the dependency of efficiency on the 2nd harmonic load. More output power can be obtained with capacitive 2nd harmonic loading with a moderate degradation on efficiency. It can be observed that Optimum Class-E conditions can be achieved over a wide range of phase angle except when the 2nd harmonic phase approaches ±180°, corresponding to a short circuit termination. Load network input port second harmonic current increases drastically as the harmonic impedance approaches the short circuit point. Achievement of Optimum Class-E conditions depends on the transistor's capability to generate a large second harmonic current components. The ultimate implementation of Class-E PA will also depend on the relative size of the grace region under particular 2nd harmonic terminations.

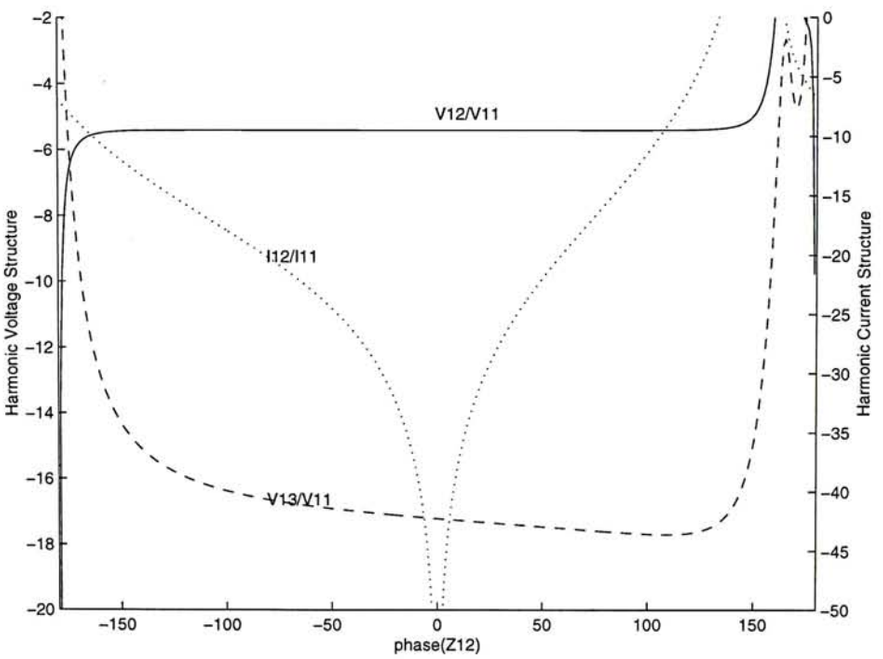
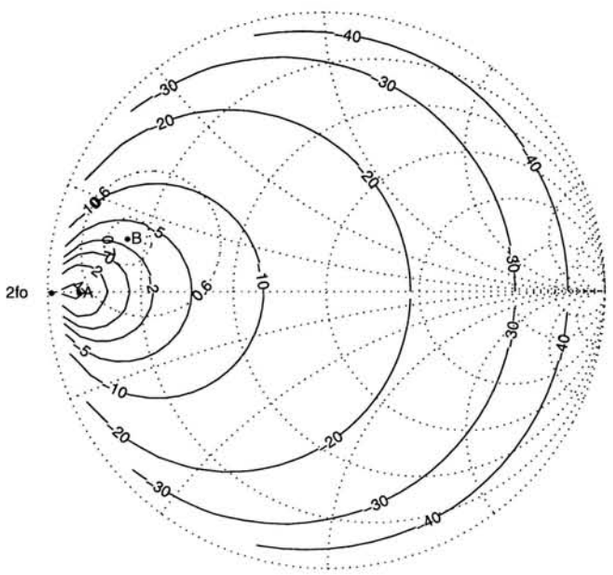


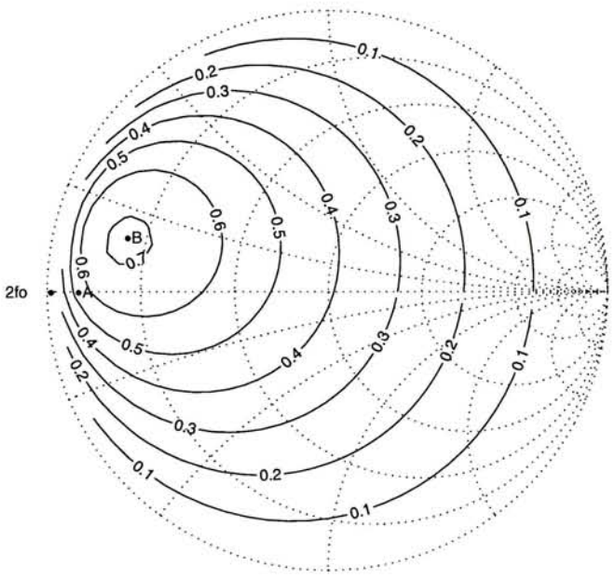
Figure 4.9 Harmonic voltage/current structure as a function of 2nd harmonic termination ($\underline{R}_{on}$=0.02)

The effects on performance contour as a function of 2nd harmonic termination is shown by a whole series of graphs in Figure 4.10. It can be observed that reactive 2nd harmonic termination offers the best efficiency with a reduced output power. High efficiency is maintained over a large grace region. On the other hand, susceptive 2nd harmonic loading delivers good output power but with very low efficiency. The grace region for efficiency is also typically very narrow. The open circuit termination offers the best compromise between power and efficiency. For Class-E operation, the short circuit point should be avoided.

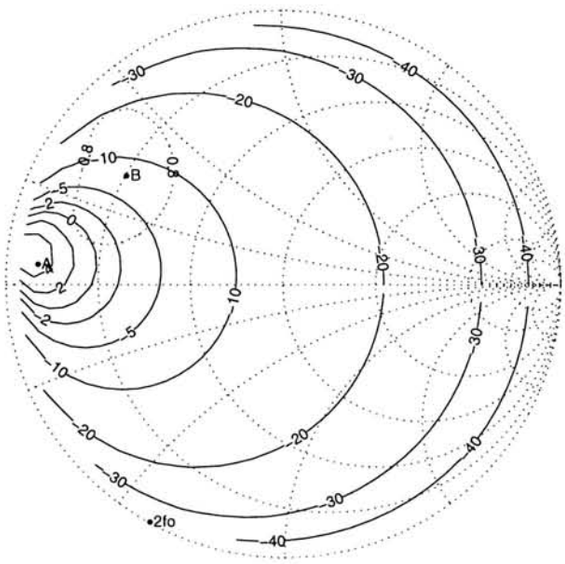
The effects of higher harmonics can also be examined similarly. However, their influences over power amplifier performances are relatively minor and will not be detailed further in this thesis.



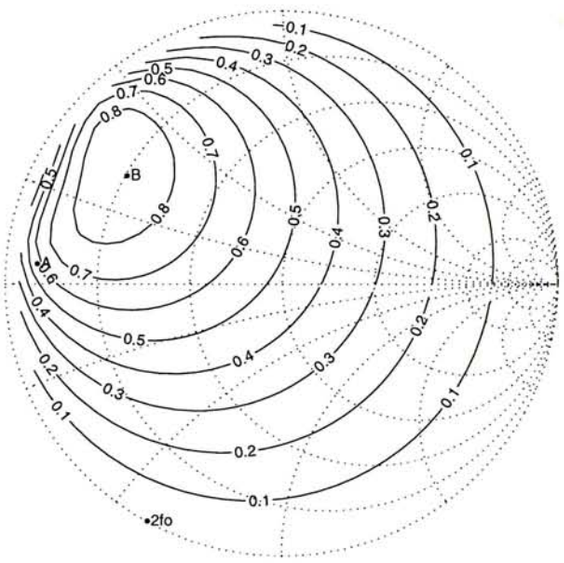
Ia) Output Power Contours[Phase(Z12)=-180]



Ib) Efficiency Contours[Phase(Z12)=-180]

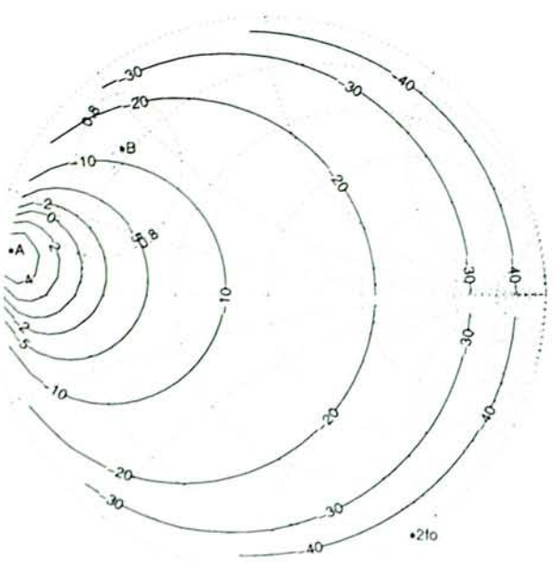


IIa) Output Power Contours[Phase(Z12)=-120]

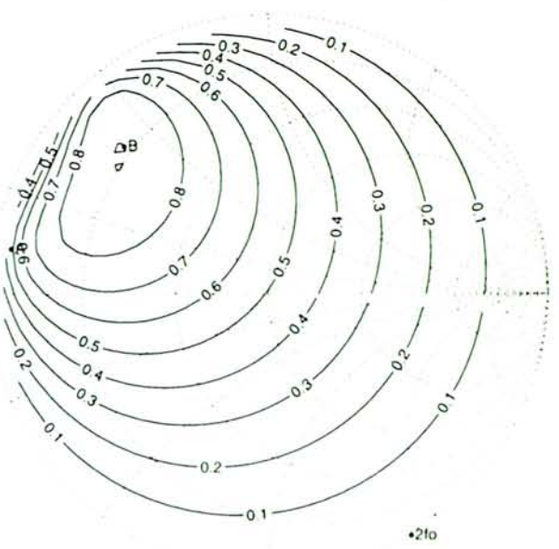


IIb) Efficiency Contours[Phase(Z12)=-120]

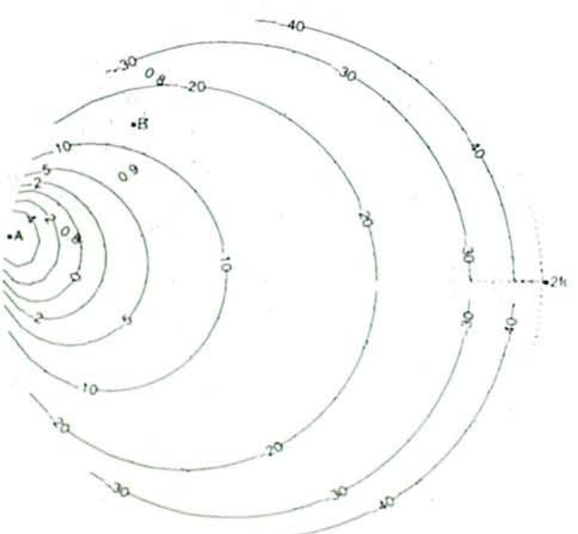
Figure 4.10 Power(dBe)/efficiency contours as a function of 2nd harmonic termination($\underline{R}_{on}$=0.02)



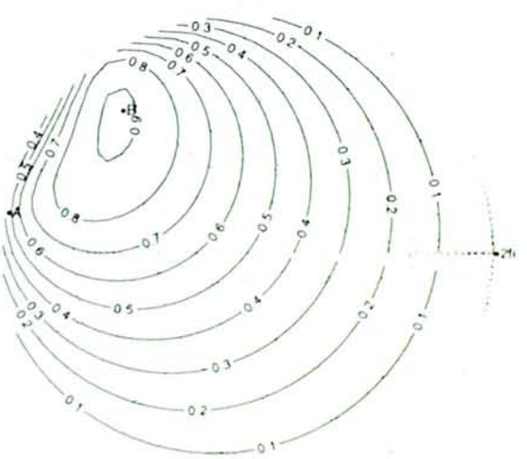
IIIa) Output Power Contours[Phase(Z12)=-60]



IIIb) Efficiency Contours[Phase(Z12)=-60]

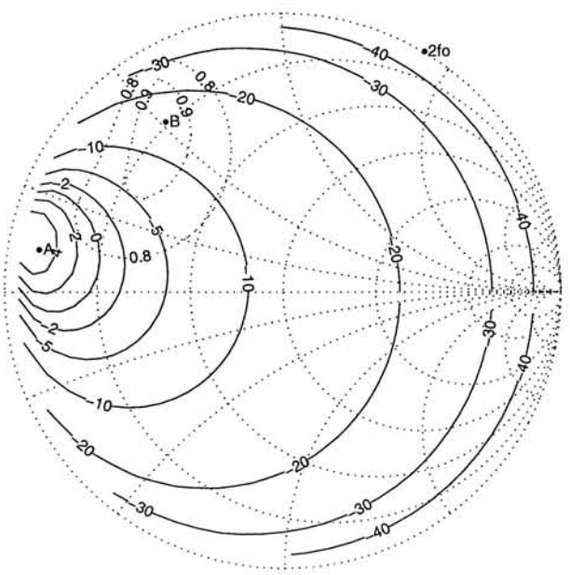


IVa) Output Power Contours[Phase(Z12)=0]

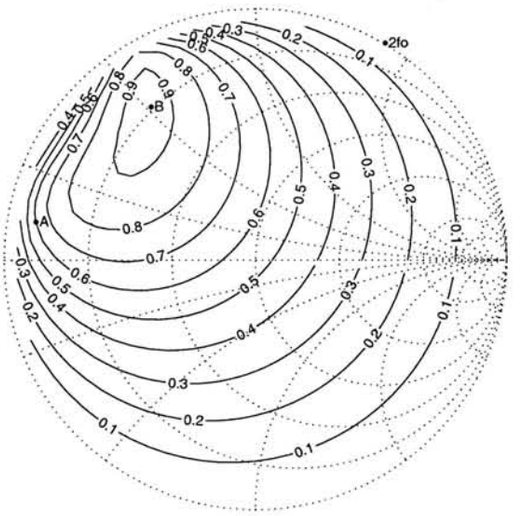


IVb) Efficiency Contours[Phase(Z12)=0]

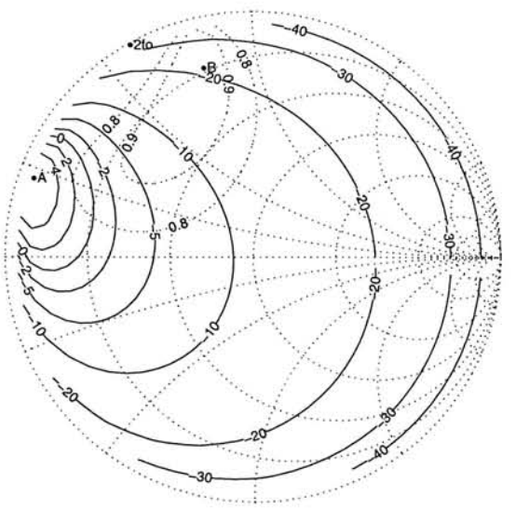
' Figure 4.10 Power(dBe)/efficiency contours as a function of 2nd harmonic termination($\underline{R}_{on}$=0.02)



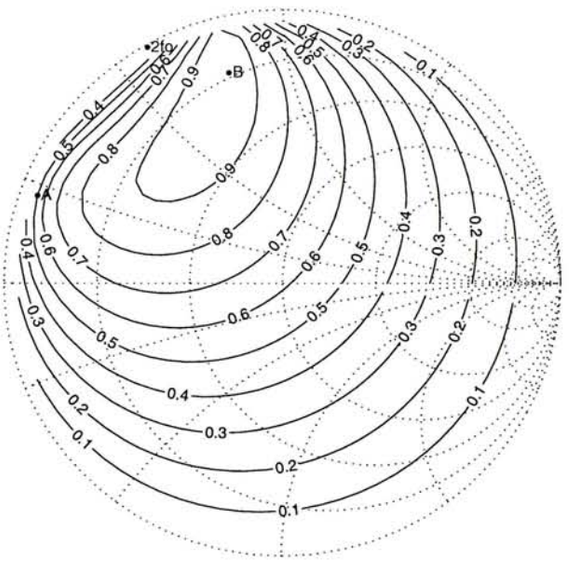
Va) Output Power Contours[Phase(Z12)=60]



Vb) Efficiency Contours[Phase(Z12)=60]



VIa) Output Power Contours[Phase(Z12)=120]



VIb) Efficiency Contours[Phase(Z12)=120]

' Figure 4.10 Output power(dBe) /efficiency contours as a function of 2nd harmonic termination(R_{on}=0.02)

4.6 Package and Other Effects

Package and other parasitic effects such as bond wire and stray capacitance can be represented as an output two-port network in between the transistor's intrinsic terminal and the transistor's physical output lead where load can be connected as shown in Figure 4.11. While theoretical predictions are made on the Transistor's Smith Chart, measurements and actual circuit design can only be accomplished on the Designer's Smith Chart. The two can be related through the transformation represented by the transistor's output two-port network.

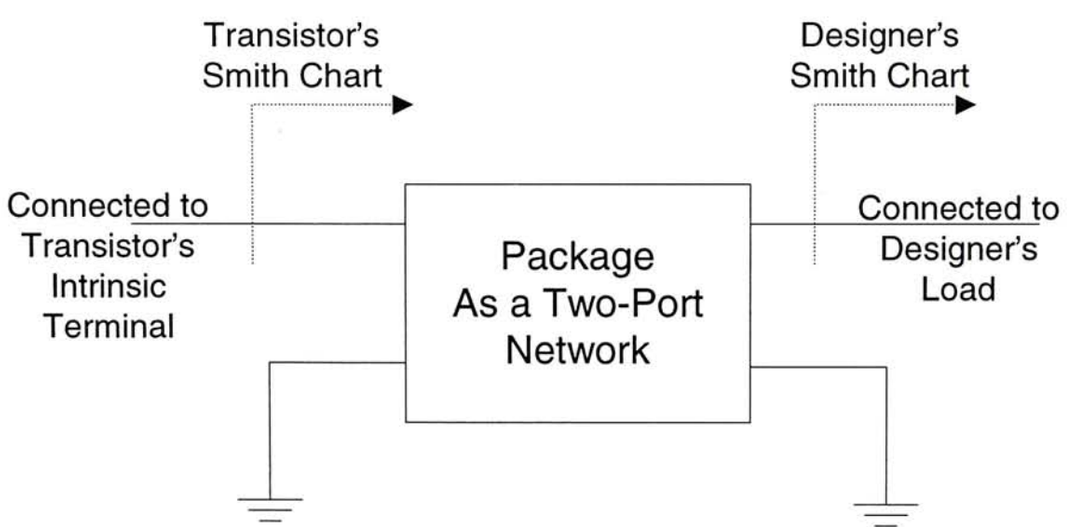


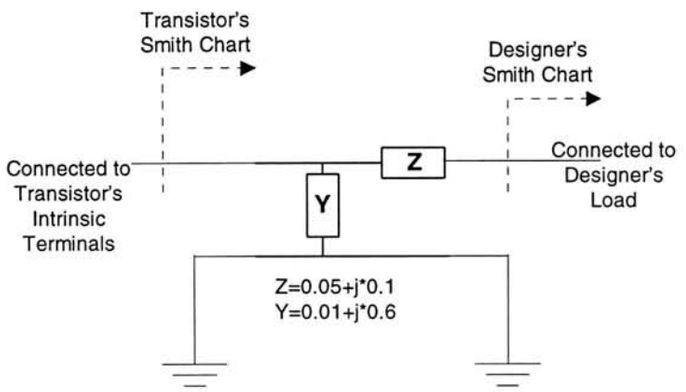
Figure 4.11 Package and parasitic effects as an output two-port network

Figure 4.12b shows how the entire Smith Chart when seen from the designer's eyes can be transformed by the two-port shown in Figure 4.12a, and perceived by the transistor's intrinsic output terminal.

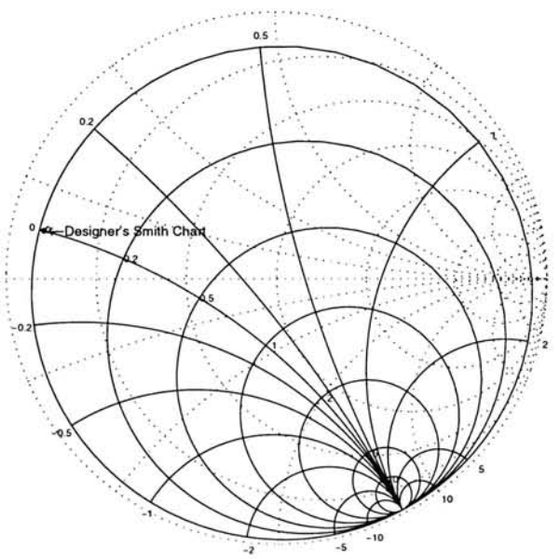
Conversely, with the same output two-port, the dash circle in Figure 4.12c represents a fictitious performance contour shown on the Transistor's Smith Chart. This performance contour appears dislocated and shrinking in size (solid circle) when perceived on the Designer's Smith Chart.

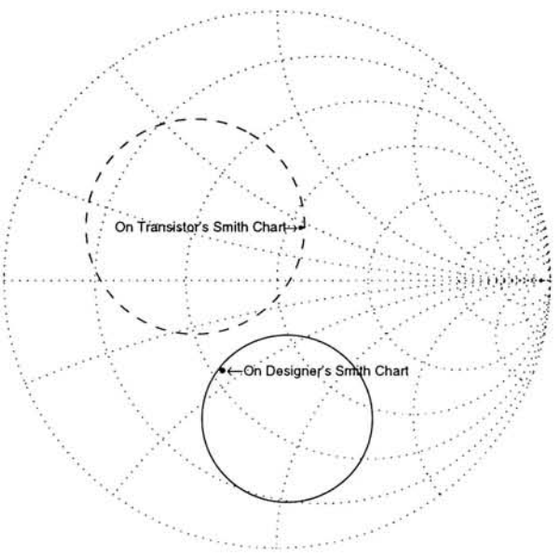
The actual transformation depends on the characteristics of the transistor's output 2-port network. For microwave power transistors, the output capacitor and bond wire represent the major parasitics at the output port. While the output capacitor has been taken as part of the transistor model in Class-E PA design, the dominant parasitic left is the bond wire, which can be modeled as a transmission line. Therefore, the Transistor's Smith Chart can be related to the Designer's Smith Chart through a simple rotation.

Other effects such as transistor input port drive, higher harmonic terminations and nonlinearity of the output capacitor all affects the ultimate performance contour in a moderate manner. For conceptual simplicity, uncertainties associated with these effects can also be absorbed into the output transformation 2-port.



a)Fictitious Output 2-port





b) Transformation of Designer's Smith Chart

c) Transformation of Performance Contour

Figure 4.12 Two-Port Network as a Transformation

4.7 Summary

In this chapter, effects such as the non-zero turn-on resistance, frequency variations, load variations and harmonic terminations and package effects have been investigated thoroughly. The results provide an indispensable aid to circuit designers.

Given a particular transistor, a knowledge of C_{out} and R_{on} allows the designer to estimate the performance bounds with regard to output power and efficiency. The operating bandwidth of the amplifier can be broadened with careful control of the amplitude and phase response of the load network. The performance contour also allows the designer to have a rough estimation of the relative ease of achieving a particular efficiency under a minimum output power requirement. For harmonic termination issues, the 2nd harmonic load should be kept away from the short circuit point to ensure proper Class-E operations. Package effects should also be taken into account for proper interpretation of the performance contours.

Effects such as device stress have not been investigated. Time waveforms of voltage/current can be obtained through inverse Fourier Transforms. Device stresses such as maximum voltage, maximum current, and the existence of negative voltage/current can be noted. Further analysis of these time waveforms for a chosen load is warranted.

With the extensive analysis results, and equipped with the capabilities for further investigation, designers can now predict, optimize and make trade-offs on Class-E power amplifer performance under general situations.

Chapter 5 Experiments

This chapter pulls together all the theoretical works into a straightforward power amplifier design procedure. Four Solid-State power amplifiers operating from 500MHz to 3.2 GHz , based upon MESFET and PHEMT devices were constructed to demonstrate the feasibility of the Class-E concept at microwave frequencies.

To begin with, two definitions regarding efficiency deserve further clarification:

1. Drain Efficiency, η_d is defined by:

$$\eta_d = \frac{P_{out}}{P_{dc}} \tag{5.1a}$$

2. Power Added Efficiency (PAE), η_{add} is defined by

$$\eta_{add} = \frac{P_{out} - P_{in}}{P_{dc}} \tag{5.1b}$$

where P_{in} = Available Power from Power Source
P_{out} = Fundamental Power delivered to Load
P_{dc} = DC power consumption of the System

Since part of the additional output power comes from an increased input power, PAE better describes the overall efficiency of the system.

The two are related by:

$$n_{add} = \left(1 - \frac{1}{G}\right) n_d \tag{5.2}$$

where G=Large Signal Power Gain of the PA

For a large gain device, the two are approximately the same. In general, high drain efficiency does not necessarily imply high PAE. High PAE does requires the pre-requisite of high drain efficiency.

5.1 Design Methods

The most popular approaches to power amplifier design are load-pull and nonlinear simulation. When nonlinear CAD tools are used, great care should be paid with regard to the accuracy and robustness of the large-signal nonlinear model of the active device. Since Class-E PA operates in a highly non-linear manner, the transistor may traverse through the cut-off region, the triode region and may even reverse conduct, the available large signal model should be able to model the operation at various possible regions. The extraction of such a model is very time consuming and requires some very expensive equipment.

Experimental load-pull, on the other hand though can be cumbersome and labor intensive, it provides accurate information regarding the nonlinear operation of the device and is adopted in this study. The load-pull set up employed in this work have been implemented through the use of tuning stubs.

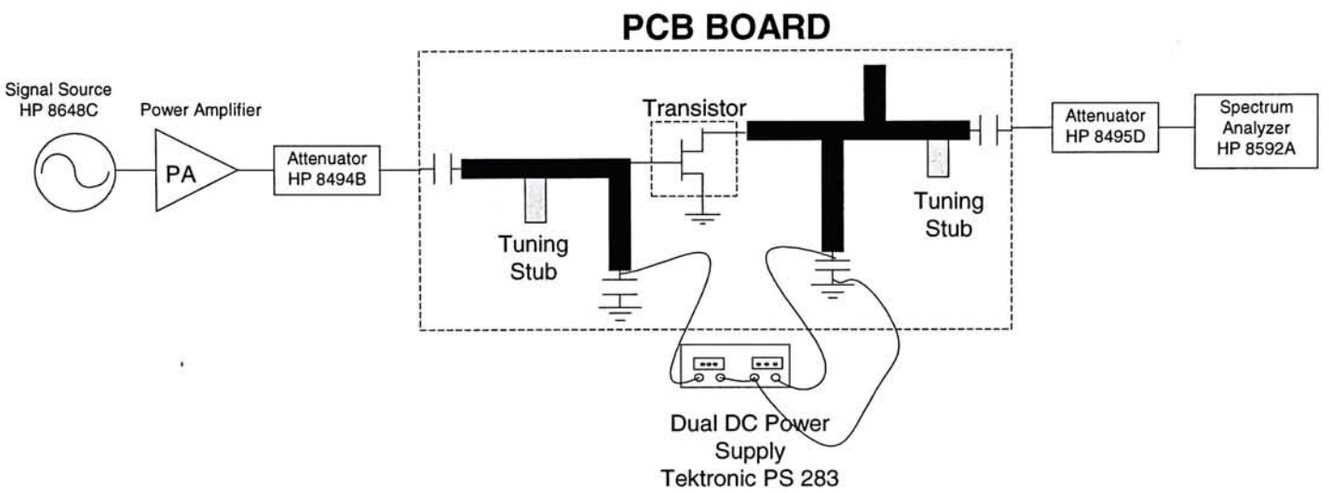


Figure 5.1 Experimental load-pull setup

Figure 5.1 shows the experimental setup for load-pull measurements used in this work. The PCB layout in the experimental setup is similar to the final circuit layout except with the presence of two tuning stubs. During load-pull measurement, both load and source impedance presented to the transistor can be varied by precision moving or cutting the tuning stubs, which are made from copper foil. The fixed circuitry in the PCB provides dc bias, harmonic impedance control and forms part of the fundamental frequency circuit. DC measurement (such as voltage and current) can be read directly from the Dual DC Power Supply or measured by additional DC voltmeters and ammeters. The spectrum analyzer serves as the power meter for measuring RF output power of the circuit. Attenuators are employed to provide power protection in case of possible oscillations. All Connection cables and attenuators are fully calibrated with a network analyzer.

5.2 500MHz Class-E PA

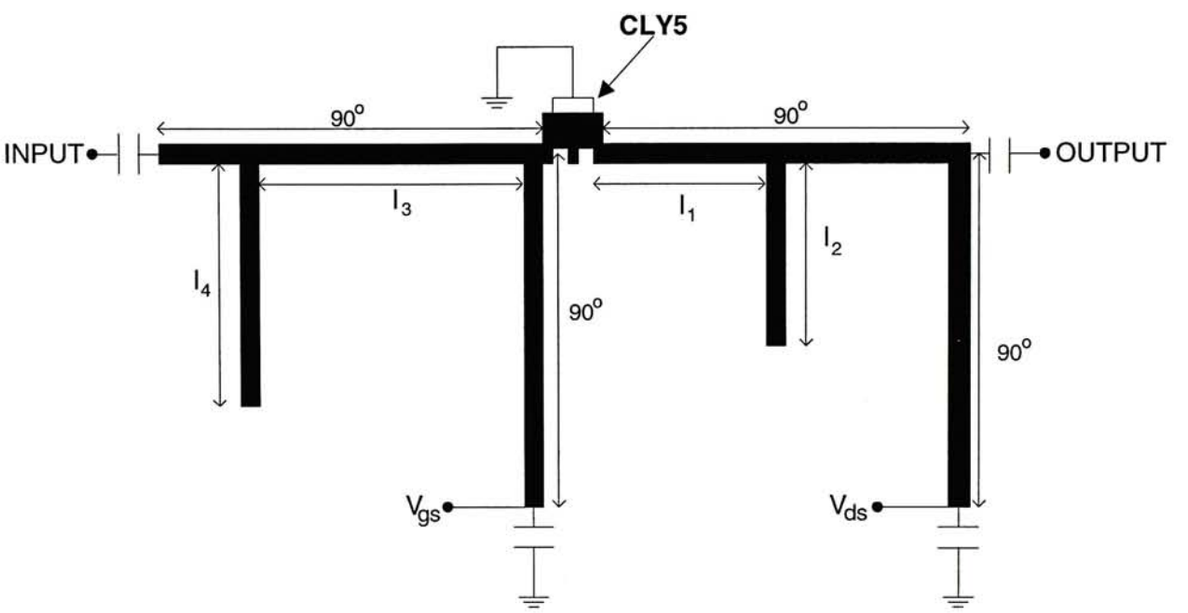


Figure 5.2 500MHz Class-E PA schematic

This experiment expands upon the work done by Z. B. Popovic in 1995[41]. Figure 5.2 shows the schematic of the PA with Siemens CLY5 MESFET as the active device. The microstrips are all 50Ω lines. Gate bias and drain bias are established through the quarter-wave shorted stubs. Input matching is done through l_3 and l_4. Output matching at fundamental frequency is done through l_1 and l_2. In theory, l_1 and l_2 are required to match the 50Ω load to the Optimum Class-E load given by (4.4b) which is re-stated below:

$$Z_{11} = \frac{V_{11}}{I_{11}} = \frac{1}{2\pi B}\left[j2\pi + (4 + j\pi)e^{-j2\tan^{-1}\frac{\pi}{2}} \right] \tag{5.3}$$

For the CLY5 MESFET, output capacitor C_{out} of 2.4pF to 2.6pF is assumed in the design. Figure 5.3 shows the optimum load impedance calculated from (5.3) as C_{out} varies from 2.4pF to 2.6pF. Also shown in the figure is the fundamental and second harmonic load impedance presented to the drain terminal as l_1 and l_2 range from 40° to 60°. It is fortunate enough that when l_1 and l_2 range from 40° to 60°, both optimum fundamental load given by (5.3) and open circuit at second harmonic can be approximately achieved simultaneously. Given the uncertainties associated with fundamental load and second harmonic load impedance, higher harmonics are ignored. Class-E operation can be approximated with proper tuning of l_1 and l_2 within the 40° to 60° range.

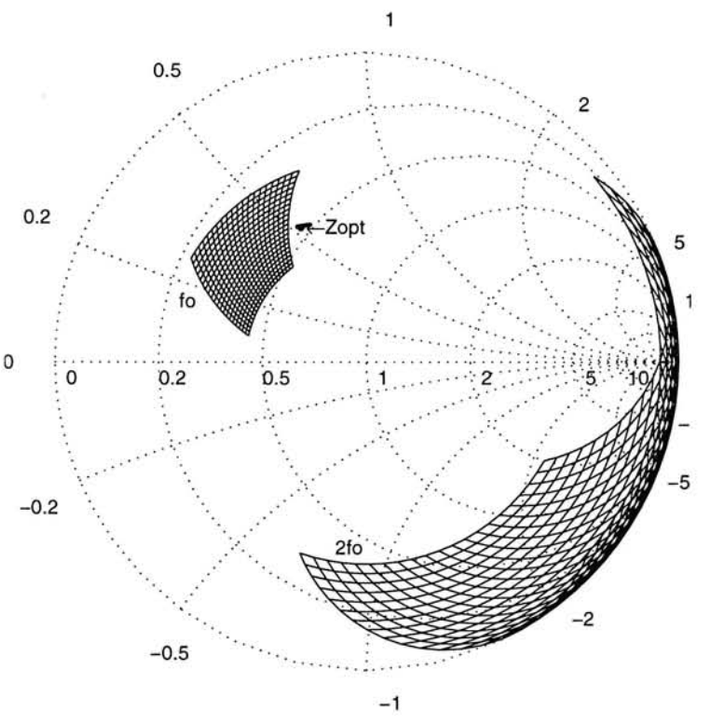


Figure 5.3 Plot of optimum Class-E load, achievable fundamental and 2nd harmonic impedance (as l_1 & l_2 vary between 40° to 60°)

In the work done by Popovic, the device was heavily saturated, and the input and output circuits were adjusted experimentally until max PAE was achieved. A maximum drain efficiency of 83 % with an output power of 550mW was claimed.[41]

In Popovic's work, only optimum design is presented. Designers have no idea of the PA performance in the neighborhood of the optimum load, with regard to the sensitivity of the optimum performance due to load variations. Should higher output power be desired, designers find no clues to trade between output power and efficiency. In this experiment, we expand upon Popovic's work by providing additional load-pull contours. Since load-pull are performed using the topology shown in Figure 5.2, the load-pull results are directly applicable to designers.

To enable complete load-pull measurement, electrical lengths of l_1 and l_2 are transformed onto the Smith Chart shown on Figure 5.4. Measurements taken at various l_1 and l_2 can then be related to the reflection coefficient on the Smith Chart. Meanwhile, arcs of constant l_1 and constant l_2 can also be used as visual matching aide to match the 50Ω load to particular load impedance required to achieve specific output power with specific efficiency shown on the load-pull contours.

During load-pull measurement, V_{ds} is fixed at 6V while V_{gs} is set at the device's threshold of –2.6V. To ensure proper operation of the active device as a switch, the transistor was heavily saturated by pumping an input power of up to 27dBm into the device. Input match was first arbitrarily set such that the device output power saturates

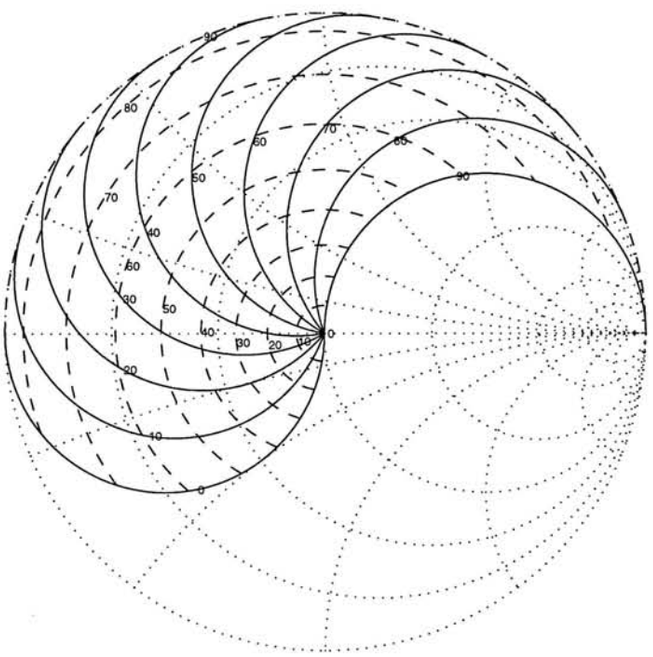


Figure 5.4 Constant l_1 & l_2 arcs on Smith Chart
(Solid line=Constant l_1 arc)
(Dashed line=Constant l_2 arc)

for most of the tuning range of l_1 and l_2. l_1 and l_2 were then varied in an increment of 5°. Output power and DC current consumption were recorded accordingly.

Figure 5.5 shows the measured output power and efficiency as a function of the input power level at a particular combination of l_1 and l_2. It is apparent that both the output power and drain efficiency saturates at high input power level. As the output power saturates while input power continues to increase, PAE exhibits a peak.

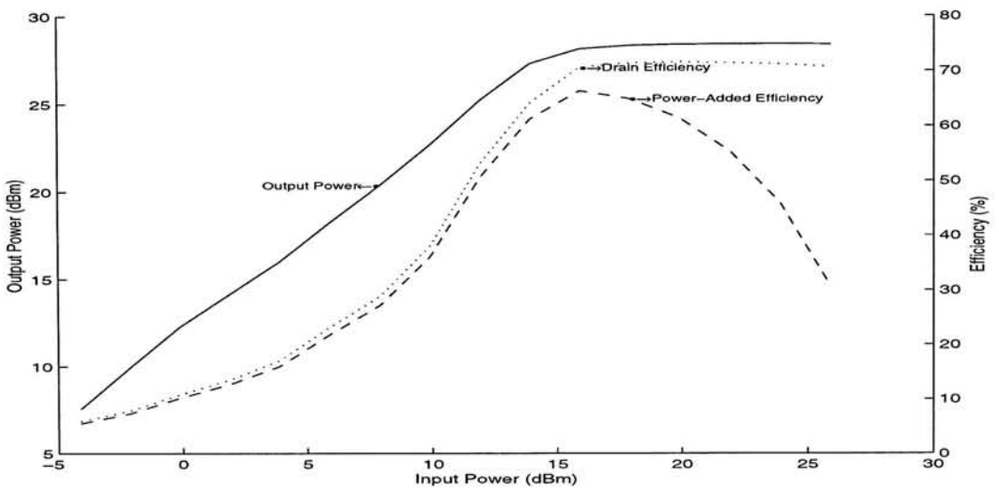
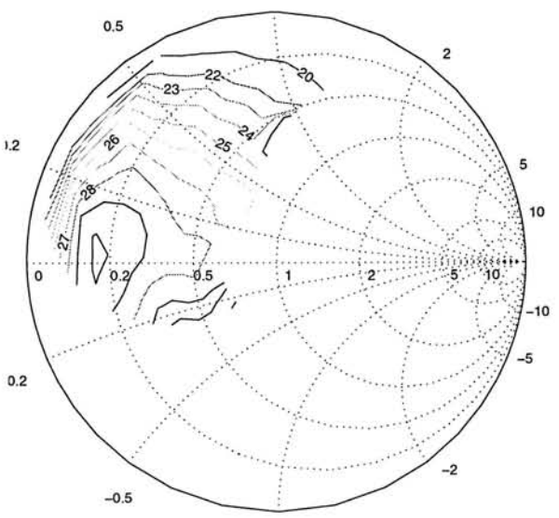
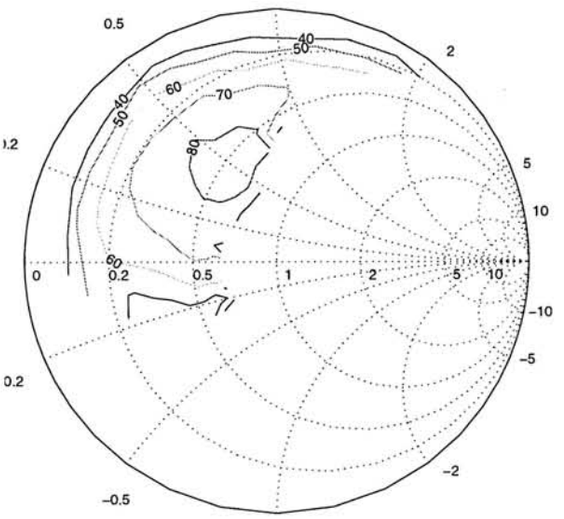


Figure 5.5 Output power and efficiency at a particular output matching condition

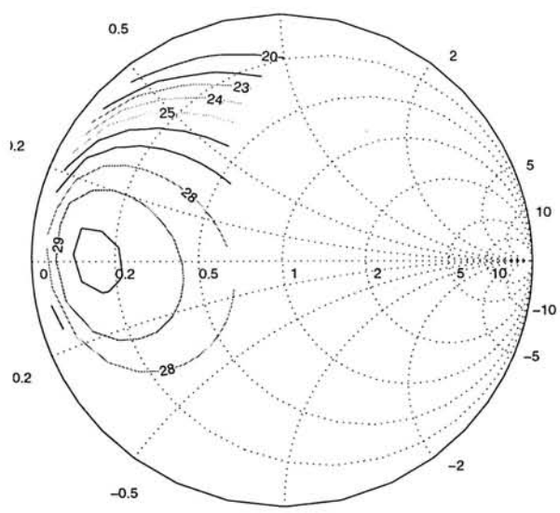
Maximum output power and maximum drain efficiency at each input power sweep were recorded as the saturated power and saturated efficiency for the particular combination of l_1 and l_2. Figure 5.6 shows the contour plots of both saturated output power and saturated efficiency as well as the theoretical prediction.



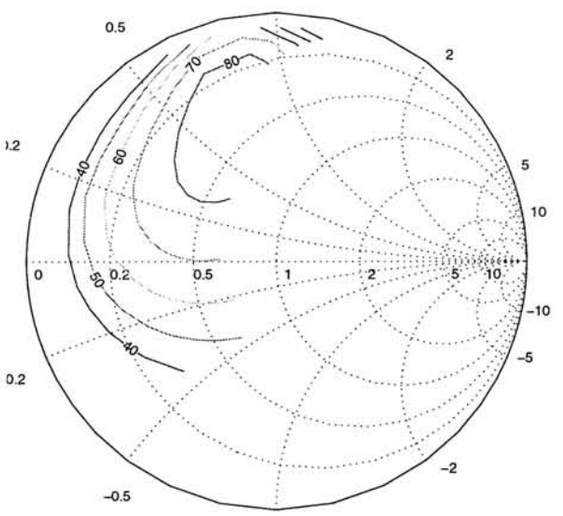
a) output power contours (measured)



b) efficiency contours (measured)



c) output power contours (predicted)



d) efficiency contours (predicted)

Figure 5.6 Power(dBm) and efficiency contours (measured and predicted)

Theoretical predictions were made with assumed values of C_{out}=2.6pF and R_{on}=4Ω. These set of values best fit the measured output power at the optimum efficiency. To

align the maximum output power contour of 30dBm on the Smith Chart, package and other parasitic effects were assumed to have perform a rotational effect on the designer's Smith Chart and the predicted contours (both output power and efficiency) were rotated by 25° counter-clockwise. By this action, the maximum efficiency contour were automatically aligned with the measurement results.

The four contour plots show good correlation between measurement and theory. The largest discrepancy exist for the over optimistic prediction of the 80% efficiency contour by theory as expected. From Figure 5.3, it is apparent that for fundamental load to go beyond the constant reactance arc of jx=0.5, the second harmonic impedance moves away from the open circuit point drastically. The problem is further complicated by the existence of package and other parasitic effects which make an accurate prediction of the second harmonic impedance presented to the intrinsic transistor very difficult, if not impossible. The shrinking of the 80% grace region depicted in Figure 5.6b is in accordance with the theoretical conclusion in section 4.5 which predicts the degradation of efficiency as a result of reduced second harmonic impedance.

With the performance contours in Figure 5.6, trade-off can be made with regard to output power and efficiency. Optimum load can be identified on the Smith Chart. The required matching circuit parameters can be directly read from Figure 5.4. Input circuit is then tuned for maximum large signal gain or for minimum return loss. If necessary, output circuit can be fine tuned in response to changes in input circuit. The process can be repeated until optimum performance such as maximum PAE is achieved.

Figure 5.7 shows the photograph of a Class-E PA designed by the above procedure, fabricated on 0.9 mm thick FR4 substrate, with ε_r of 4.1. The output circuit is selected within the 80% efficiency contour. No efforts are made to optimize the output power. Finally, the input circuit is tuned for maximum gain. The output performance is shown in Figure 5.8. The PA demonstrates a saturated output power of 25.6 dBm, with 85% maximum drain efficiency and 79% maximum power added efficiency.

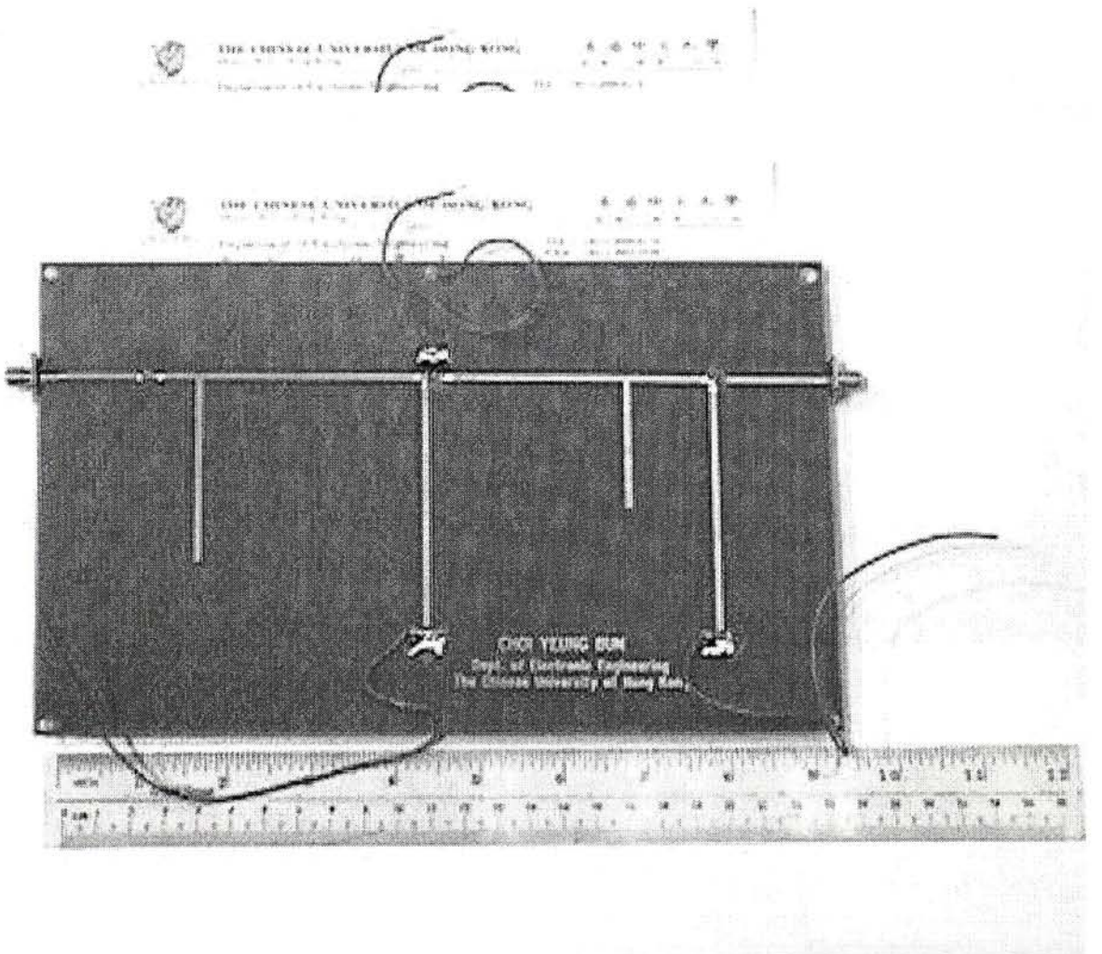


Figure 5.7 Photograph of the 500MHz Class-E PA fabricated on 0.9mm thick FR4 substrate with ε_r = 4.1

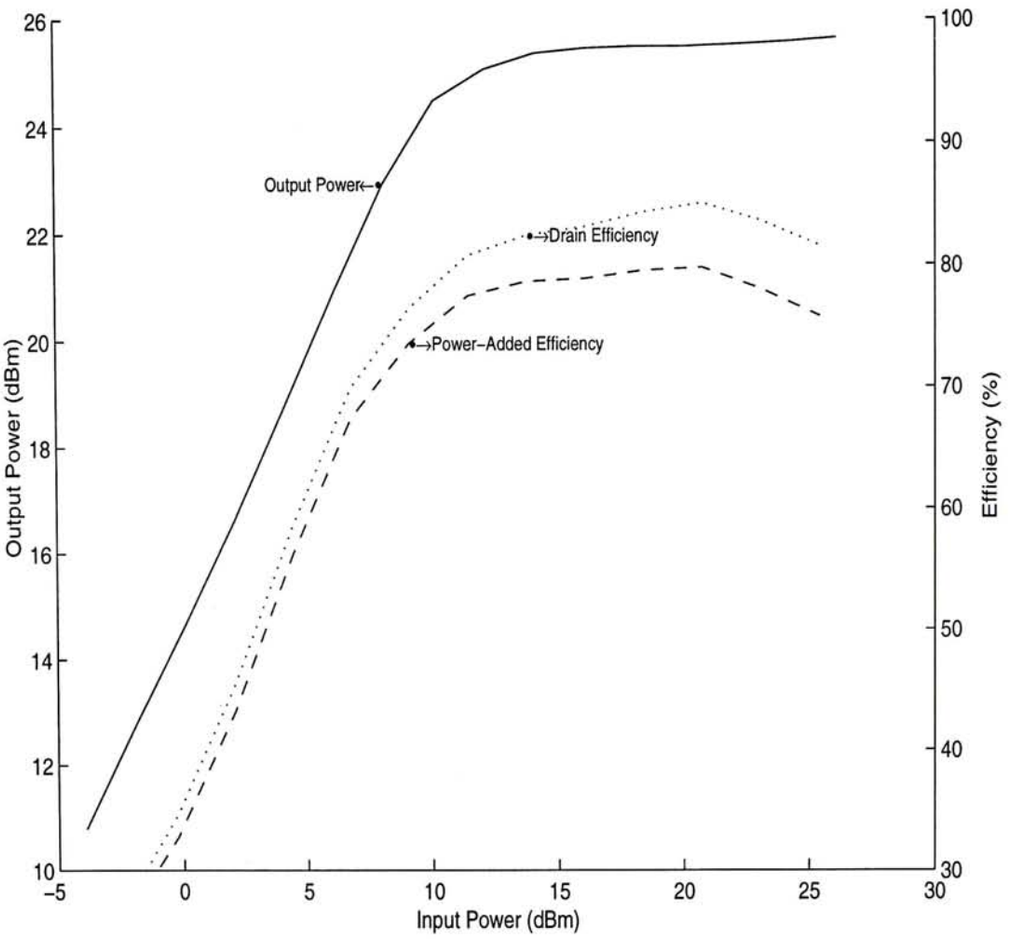


Figure 5.8 Amplifier output power and efficiency for the 500MHz Class-E PA fabricated on 0.9mm thick FR4 substrate with ε_r = 4.1

5.3 1.8GHz PHEMT Class-E PA

Recent advances in solid-state technology leads to the development of a large number of high performance devices, enabling the design of next generation high efficiency, high frequency power amplifiers possible. HBT and HEMT have emerged as valuable devices for microwave and mm-wave applications. This experiment report on the Class-E PA operation employing PHEMT as the sole active device.

While PHEMTs share similar electrical characterisitcs as MESFETs, distinctive dissimilarities exist. The most striking aspect concerning large signal operation lies in the basic I-V curves. The maximum attainable drain-source current for PHEMTs can be as much as 75-100% above I_{DSS}. In contrast, MESFETs might show only 20-25% above I_{DSS} with the same forward gate bias. Because of the shift in maximum output current, standard guidelines for PA design such as that given in [42] & [43] may have to be modified accordingly. A detailed investigation of the device's salient features and their associated implications on circuit operations, with regard to the I-V characteristics, g_m profiles and high frequency behaviors can be found in numerous literature[44],[45].

Figure 5.9 shows the schematic of the 1.8GHz PHEMT Class-E power amplifier. The active device used is a 0.25μm PHEMT from Filtronic, LP1500P100. To simplify the design process, all microstrips are 50Ω lines. Gate bias and drain bias are brought through the quarter-wave shorted stubs. While these quarter-wave shorted stubs are transparent at the fundamental frequencies, they have profound effects on the second harmonic impedance. Independent studies by M. Maeda[46], K. Jeon[47]and P.M.

White[48] concluded that suppression of source 2nd harmonic voltage help reduces asymmetric distortion of the gate-source driving waveform which results from gate-source non-linear input capacitance inherent in FET. Symmetric drive is crucial to proper timing of transistor turn-on and turn-off and hence proper suppression of source 2nd harmonic voltage is conducive to efficiency enhancement as a result. Degree of drive distortion depends on the relative non-linearity of C_{gs}. C_{gs} of typical PHEMT shows a deep dependence on V_{gs}, hence short-circuiting source 2nd harmonic impedance is expected to produce profound effects on efficiency enhancement especially for PHEMT devices[48]. For this reason, the quarter-wave shorted stub, s_1 is brought to the gate as closely as possible to short-circuit the source 2nd harmonic impedance.

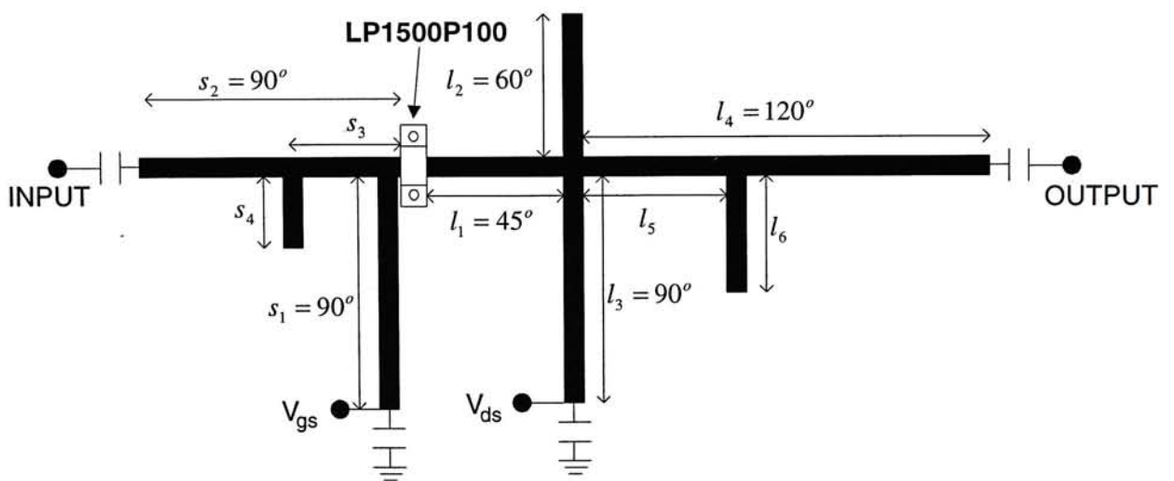


Figure 5.9 1.8GHz PHEMT Class-E PA schematic

In contrast to the circuit in Figure 5.2, explicit load 2nd harmonic impedance control is accomplished through l_1 and the biasing stub l_3 . In this arrangement, open circuit at load 2nd harmonic impedance is ensured irrespective of fundamental load tuning. This prevents possible degradation on efficiency grace region due to 2nd harmonic impedance mismatch

as observed in section 5.2.

While both source and load 2nd harmonics are well under controlled, fundamental input/output matching are accomplished through s_3 , s_4 and l_2 , l_5 & l_6. Figure 5.10 shows the arcs of constant l_5 & l_6 overlaid on the Smith Chart, in relation to the fundamental load impedance seen from the transistor drain terminal. The location of the marked point where all constant l_5 & l_6 arcs converge to is controlled by l_1 & l_2. While l_1 is set by load 2nd harmonic requirement, l_2 is chosen so as to bring the convergence point to where optimum load is expected. For the LP1500P100, estimated C_{out} of 0.3pF to 0.5pF is assumed with an approximate value of R_{on} of 1~2 Ω. Optimum load can be calculated from (5.3). To allow greater tuning range, l_2 is set to 60°. Experimental adjustments can then be carried out in the neighborhood of the convergence

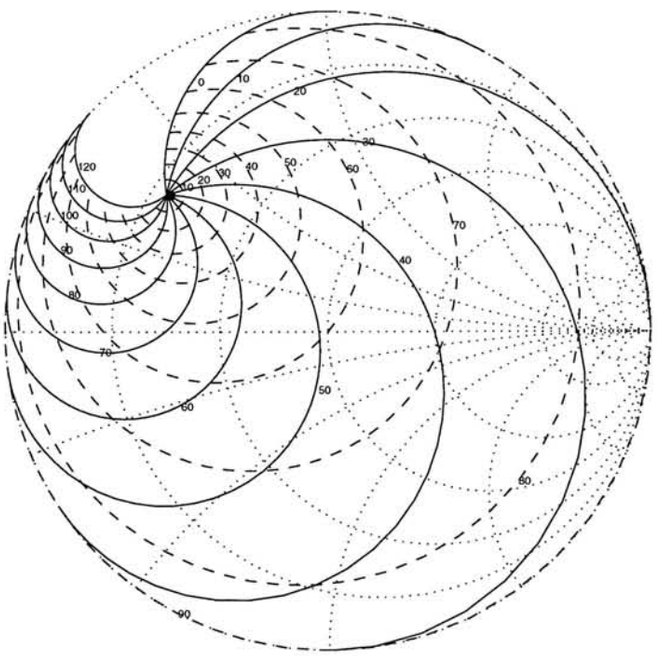
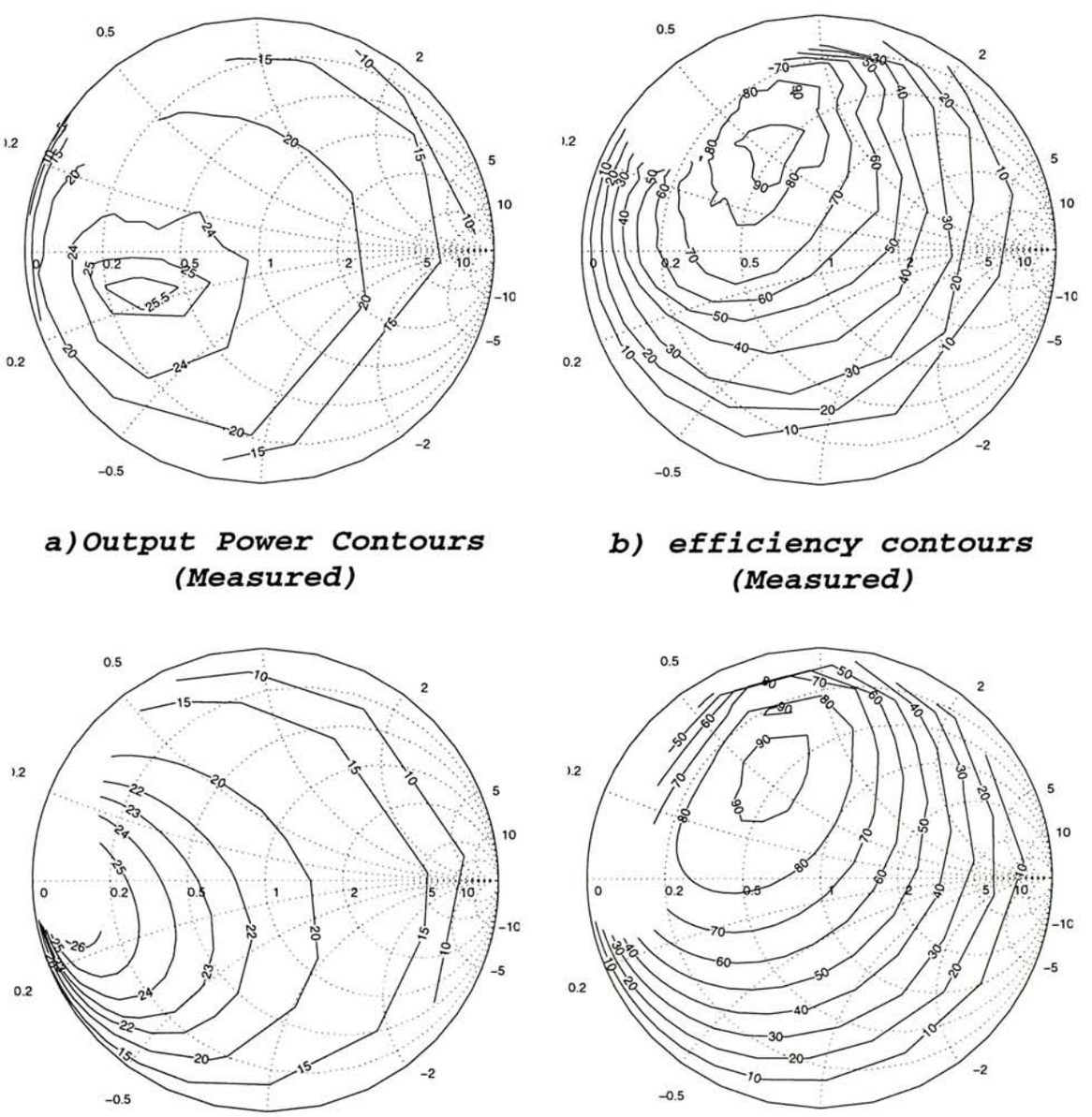


Figure 5.10 Constant l_5 / l_6 arcs on Smith Chart
(Solid line=Constant l_5 arc)
(Dashed line=Constant l_6 arc)

point until objective of optimum efficiency is achieved.

To reveal more vital information of the power amplifier, extensive load-pull measurements were taken in this experiment. The transistor was biased at pinch off with V_{ds}=3V and Ids=5mA (~5% of I_{MAX}). The load-pull procedure described in section 5.2 was repeated here with l_5 and l_6 varied in an increment of 5°. Figure 5.11 shows the performance contour with the



a)Output Power Contours (Measured)

b) efficiency contours (Measured)

c) Output power contours (modeled)

d) efficiency contours (modeled)

Figure 5.11 *Power(dBm)/efficiency contours (Measured /modeled)*

theoretical prediction in parallel.

To best fit the maximum output power, C_{out}=0.42pF and R_{on}=2.2Ω were assumed in the modeled contours calculation. To account for package and other output port parasitic effects, the theoretical performance contours were rotated counter clockwise so as to align with the measured maximum output power point. By this alignment, the modeled efficiency contour closely resembles that of measurements without any additional adjustments.

The final circuit was then fabricated on 0.8mm (31 mil) thick Duriod 5870, with ε_r =2.33 . The output circuit was selected within the 90% drain efficiency contour, with a saturated output power of 21dBm. To facilitate the design process, input match was tuned for maximum power gain at low input power level. A photograph of the final circuit is given in Figure 5.12.

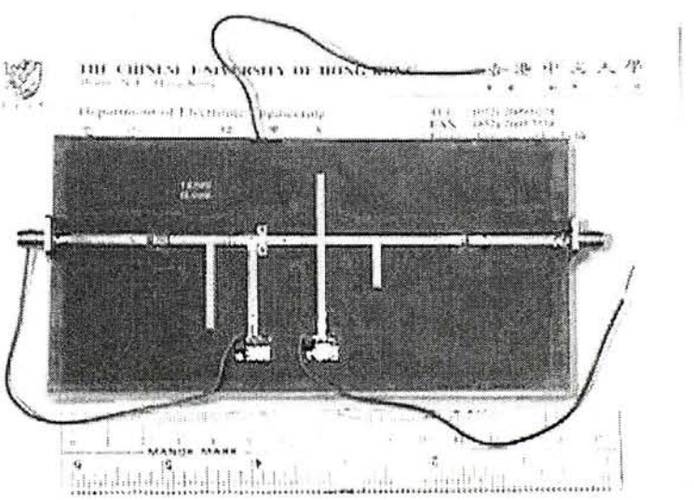


Figure 5.12 Photograph of the 1.8GHz Class-E PA fabricated on 0.8mm thick Duroid 5870 substrate with ε_r = 2.33

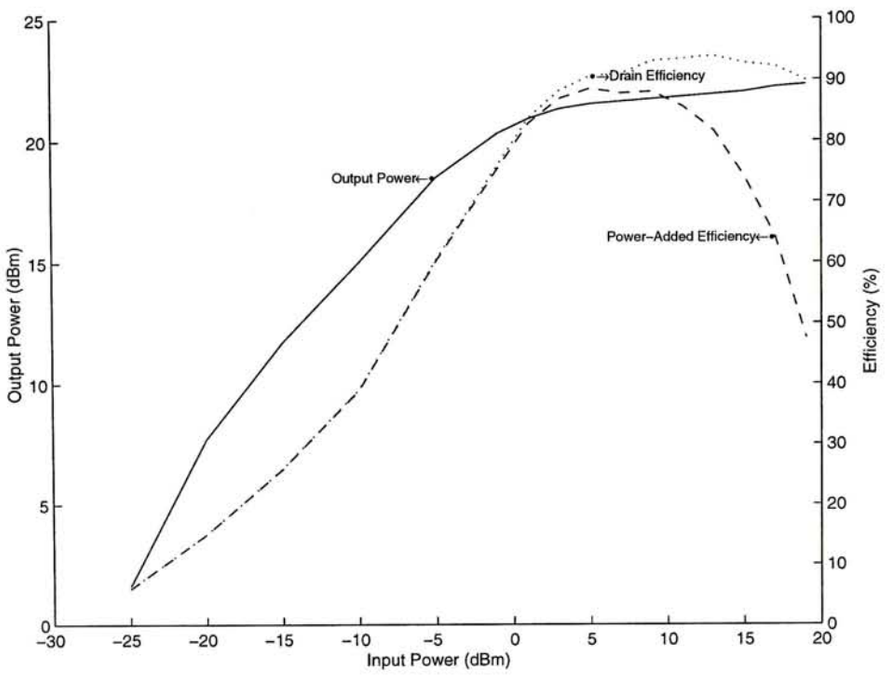


Figure 5.13a *Output power and efficiency of the 1.8GHz Class-E PA*

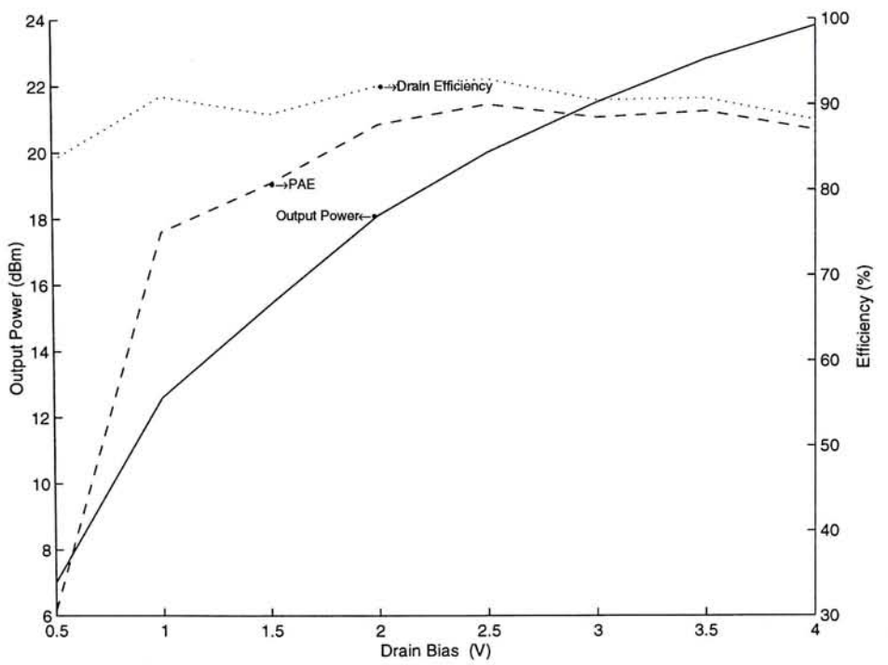


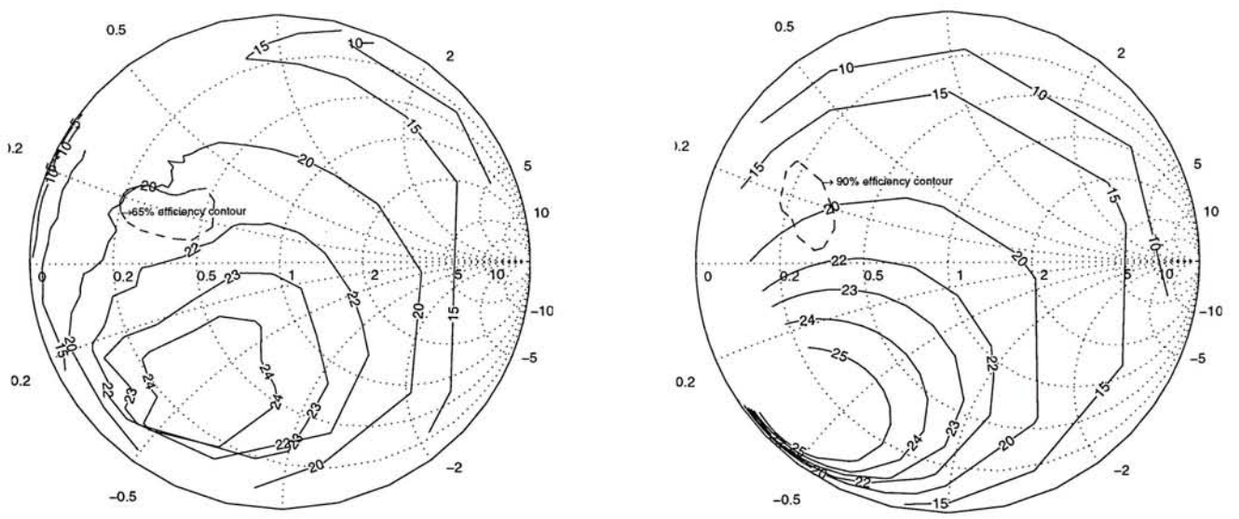
Figure 5.13b *Output power and efficiency versus drain biasing voltage (input power = 5dBm)*

Figure 5.13a shows the output power and efficiency at the nominal drain bias of 3V. The amplifier exhibits a maximum saturated power of 22dBm, with maximum drain efficiency of 93% and maximum PAE of 88%.

Figure 5.13b shows the output power as the drain bias varies. The output power shows typical square law dependency on drain bias voltage as indicated by (4.5). It is interesting to note that the drain efficiency of true Class-E operation is relatively less insensitive to bias variation. The reason is that optimum Class-E load is determined independent of the supply voltage [see (4.4)] as opposed to other classes of operation[42],[43]. This property can be further exploited for direct drain bias modulations using amplitude cancellation and restoration technique.

5.4 3.2GHz PHEMT Class-E PA

The 3.2 GHz PHEMT Class-E PA is a frequency scaled version of the 1.8GHz PA described in the previous section. DC bias was maintained at V_{ds}=3V with I_{ds}=5mA. Figure 5.14a shows the saturated output power contour with the 65 % drain efficiency contour superimposed on the same figure. Idealized performance contours using derived quantities of C_{out}=0.42pF and R_{on}=2.2Ω were shown in Figure 5.14b. The calculated performance contours were first counter-clockwise rotated so as to align with the measured maximum output power point.



a) Output power / efficiency contours (Measured)

b) Output power / efficiency contours (predicted)

Figure 5.14 Output power(dBm) / efficiency contour (Measured / Predicted)

The measured drain efficiency ranges from about 65%~70%. This is the maximum attainable efficiency with the fundamental tuning circuit shown in Figure 5.9. Although 60%~70% represents a very high efficiency at microwave frequencies, theoretical prediction shown in Figure 5.14b indicates that a higher efficiency should be attainable. Performance degradation is mainly due to harmonic mismatch.

Although explicit 2nd harmonic open circuit is ensured at the drain terminal as shown in Figure 5.9, harmonic mismatch can still result due to distortions from package and other output port parasitics, especially at high frequencies. From Figure 4.8-4.10, it is obvious that reduction in efficiency can result from capacitive load (2nd harmonic) termination. Although higher harmonic mismatches can also cause decrease in efficiency, their effects are relatively insignificant and will be ignored here[49],[50].

To bring the capacitive load (2nd harmonic) impedance back to the open circuit point, the 2nd harmonic compensation line l_1 (refer to Figure 5.9) has to be shortened. The fundamental output matching circuit l_5 and l_6 will then have to be modified accordingly.

A new 3.2 GHz PA circuit was fabricated with l_1 shortened by 15°, i.e., l_1=30°. The fundamental output matching circuit l_5 and l_6 were then re-adjusted in the optimum efficiency region as indicated in Figure 5.14. Input circuit was then tuned for maximum power gain at low input power level. Figure 5.15 and Table 5.1 compare the performance of the two 3.2GHz PAs with and without load 2nd harmonic re-adjustment.

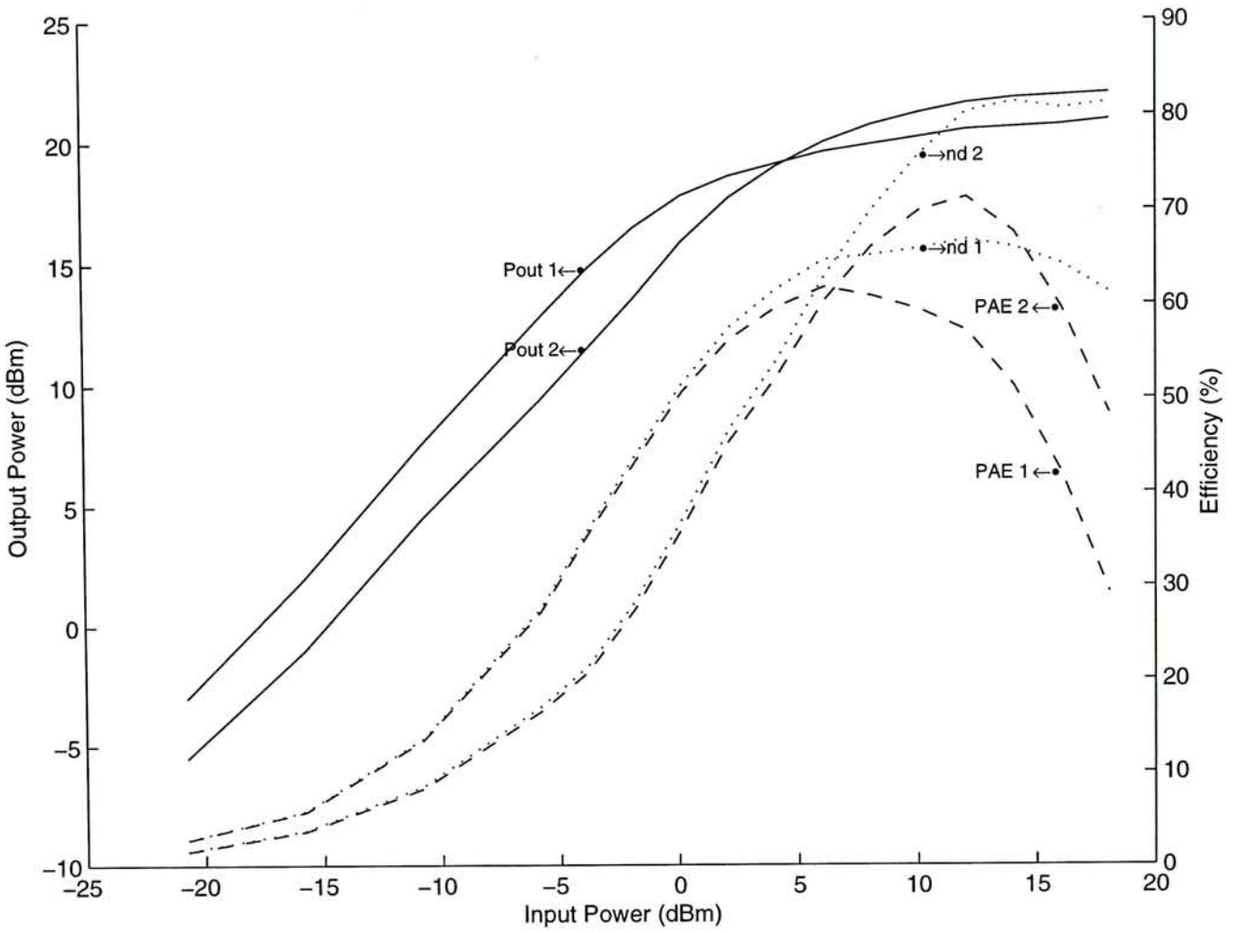


Figure 5.15 Amplifier output power and efficiency
(1.....without load 2nd harmonic re-adjustment)
(2.....with load 2nd harmonic re-adjustment)

Table 5.1 Comparison of PA performance with and without load 2nd harmonic re-adjustement.

	Without load (2nd harmonic) re-adjustment	With load (2nd harmonic) re-adjustement	Improvement
Maximum Output Power (dBm)	20.9	22	1.1
Maximum Drain Efficiency (%)	66	81	15
Maximum PAE (%)	61	71	10

Tremendous improvements have been achieved by re-adjusting the load (2^{nd} second harmonic) impedance. Observations show that the biasing circuit, the matching circuit for both fundamental and 2^{nd} harmonic frequencies are all vital for high power/efficiency operation.

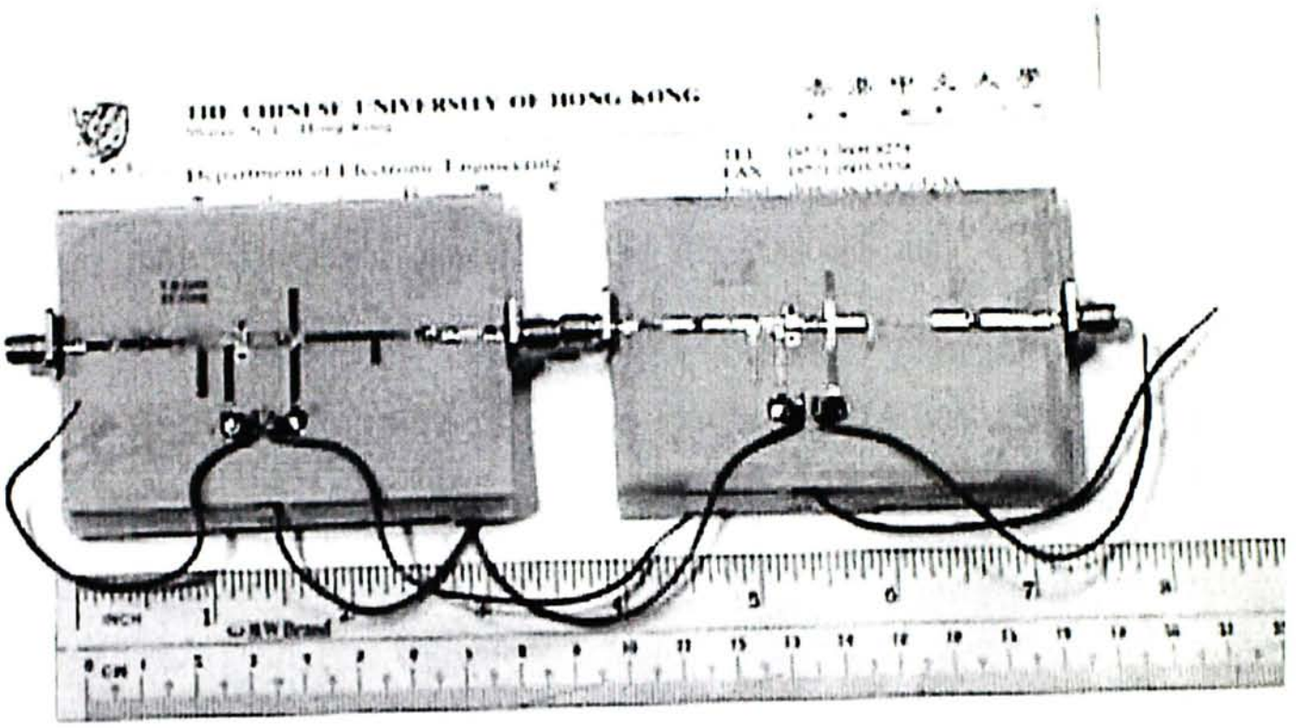


Figure 5.16 Photographs of the two 3.2GHz Class-E PAs
(left---without 2nd harmonic readjustment)
(right-with 2nd harmonic readjustment)

5.5 Conclusions

This chapter make extensive application of the theoretical guideline developed in earlier chapters in the process of designing 4 solid-state power amplifiers. State-of-the-art efficiency of around 80%-90% were achieved from 500MHz up to 3.2 GHz. The 4 circuits show vivid illustration on application of the Class-E concept towards high efficiency microwave power amplifier design. Even though only 4 circuits were demonstrated, the design procedure is generic and designers can easily adapt it to their own applications.

Chapter 6 Conclusion and Recommendation for Future Work

6.1 Conclusion

This thesis describes the analysis, synthesis and optimization of high efficiency microwave power amplifiers based upon the Class-E concept.

Previous reports on Class-E circuit analysis was mainly being carried out in time-domain. This approach suffers from complicated set of non-linear time equations which are difficult to solve and understand. Besides, the analysis is only applicable to specific topology under specific implementation method. The complexity of algebra involved limit the use of Class-E circuits to a few very simple topology choice. Furthermore, incompatibility with frequency domain conventions in microwave community confined Class-E development to low frequency applications.

Major contributions of this work include:

- Development of a general frequency domain analysis method based on the harmonic balance principle for analyzing arbitrarily Class-E circuit independent of topology choice and method of implementation.

- Formulation of the Class-E concept in frequency domain, in conjunction with the idea of harmonic tuning and waveform shaping towards high frequency high efficiency amplification.

- Direct optimization of circuit performance by exploiting the special structuring of the

new formulation. Both analytical and numerical solutions for optimum Class-E operations were derived.

- Extensive performance evaluations of Class-E circuit subject to various circuit parameter variations, such as finite turn-on resistance, frequency shift, load variations, harmonic loading and package effects.

- Transform all theoretical works into a straightforward power amplifier design procedure. Four solid-state power amplifiers operating from 500MHz to 3.2GHz were constructed as a vivid illustration of the design procedure. State-of-the-art efficiency of around 80%-90% were achieved.

6.2 Recommendation for Future Work

- Further efficiency enhancement can be achieved through explicit 3rd harmonic impedance control. Designer should know what's to gain by terminating higher harmonic impedances in order to decide if extra performance is worth the extra complication.

- Circuits other than amplifiers can also be studied. Frequency multiplier operation is feasible with proper control of fundamental output current. High efficiency oscillator may also be investigated with explicit feedback circuitry.

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